

FIG. 1

FIG. 2(a) FIG. 2(b)

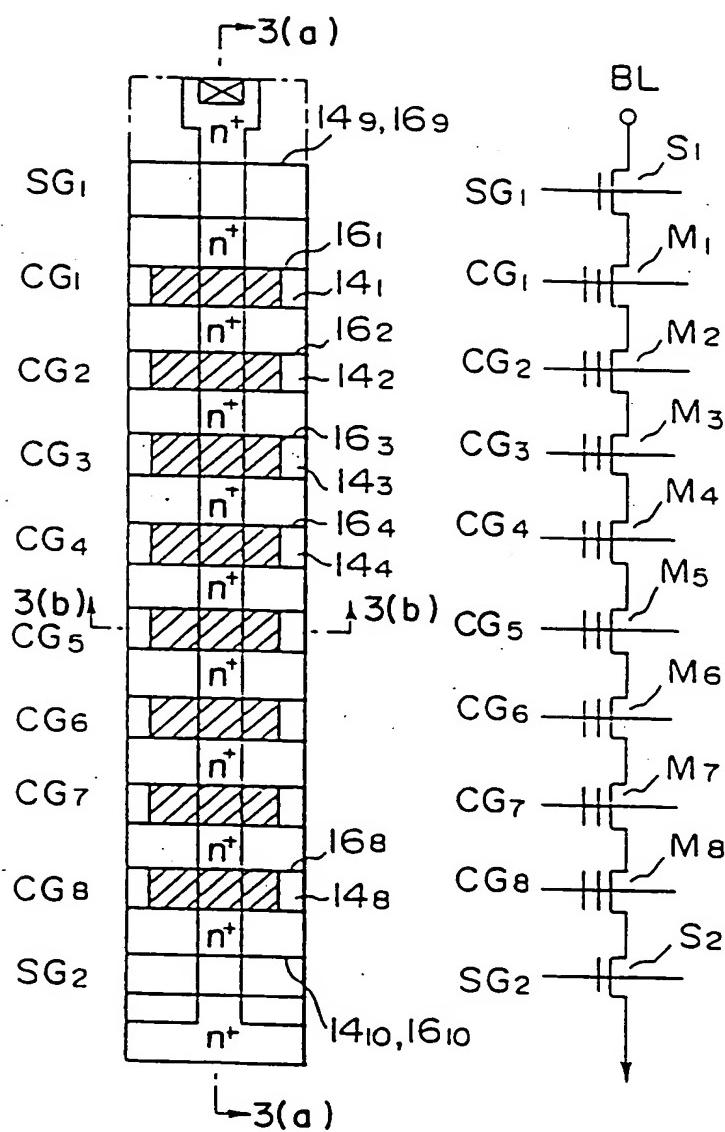


FIG. 3(a)

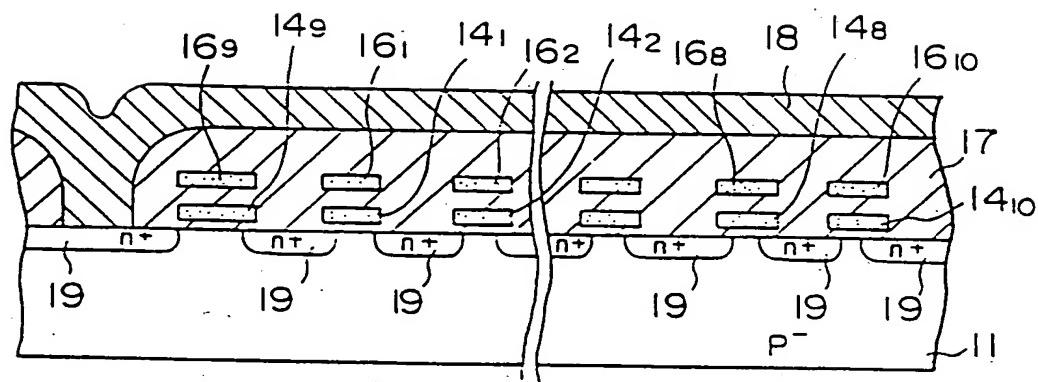
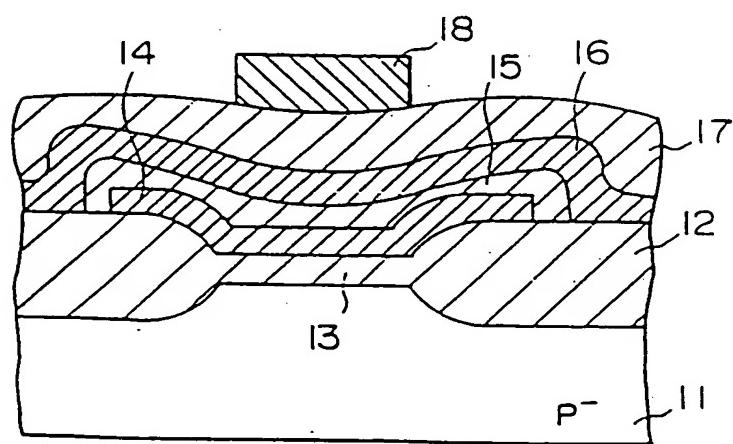


FIG. 3(b)



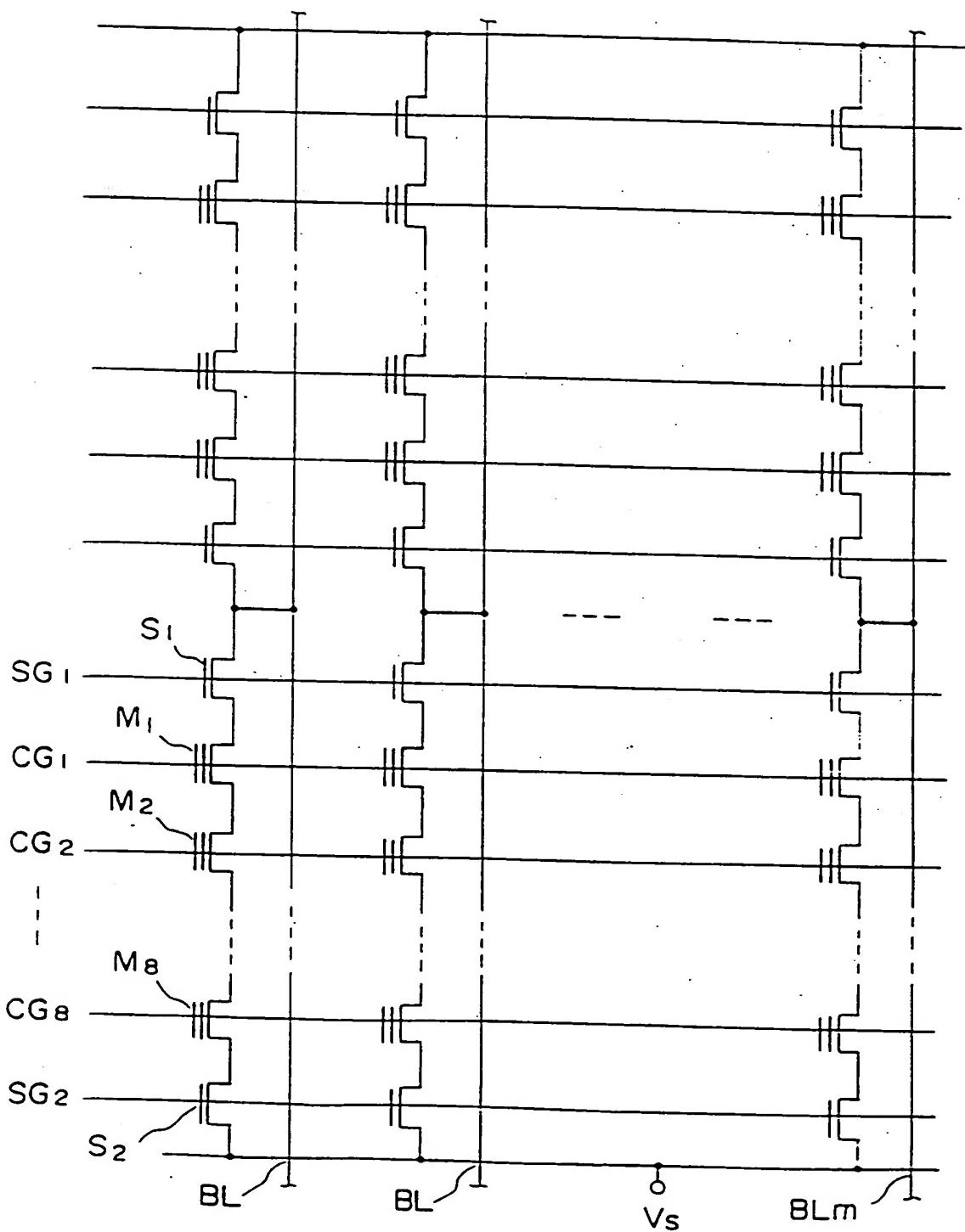


FIG. 4

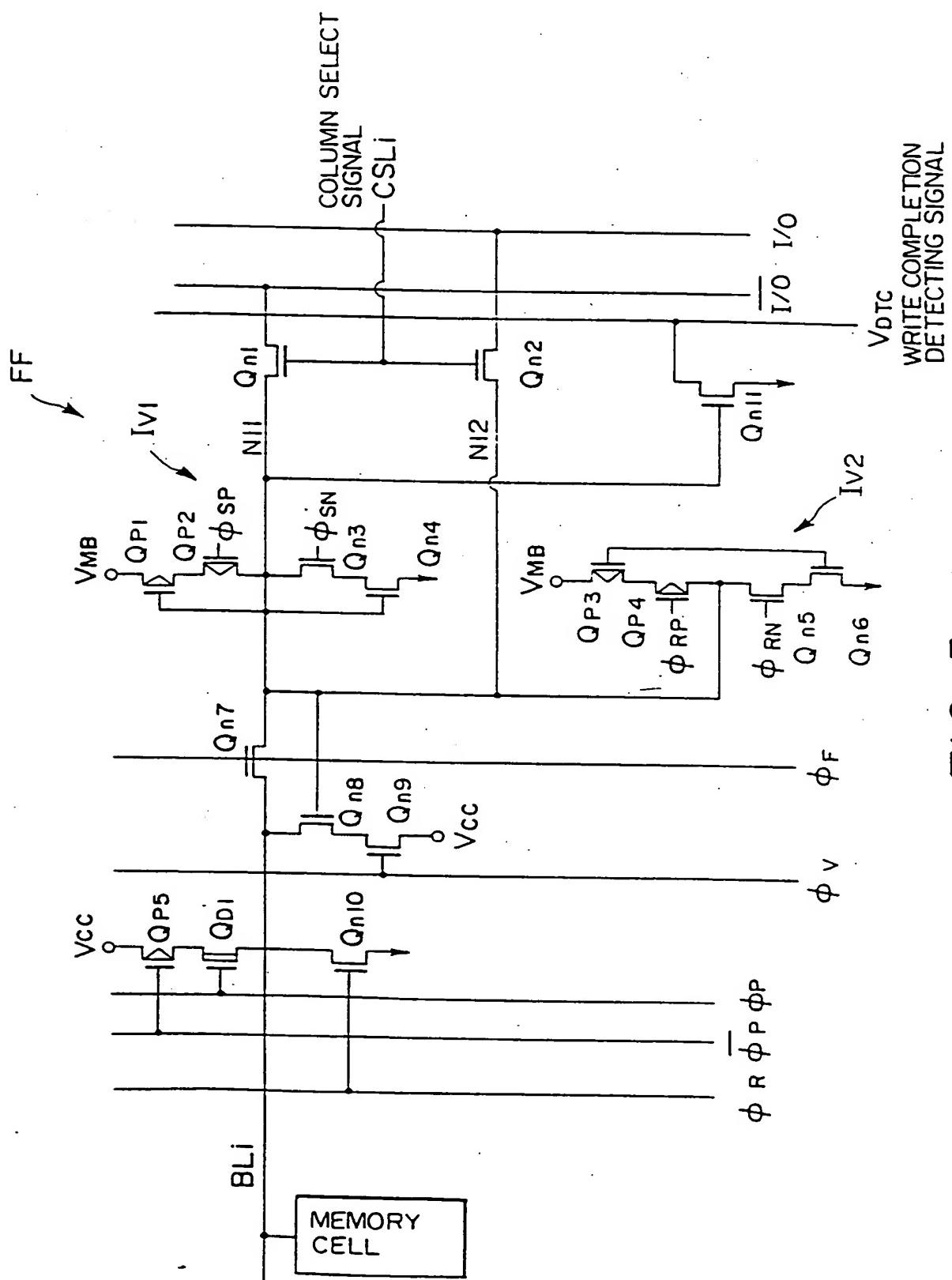


FIG. 5

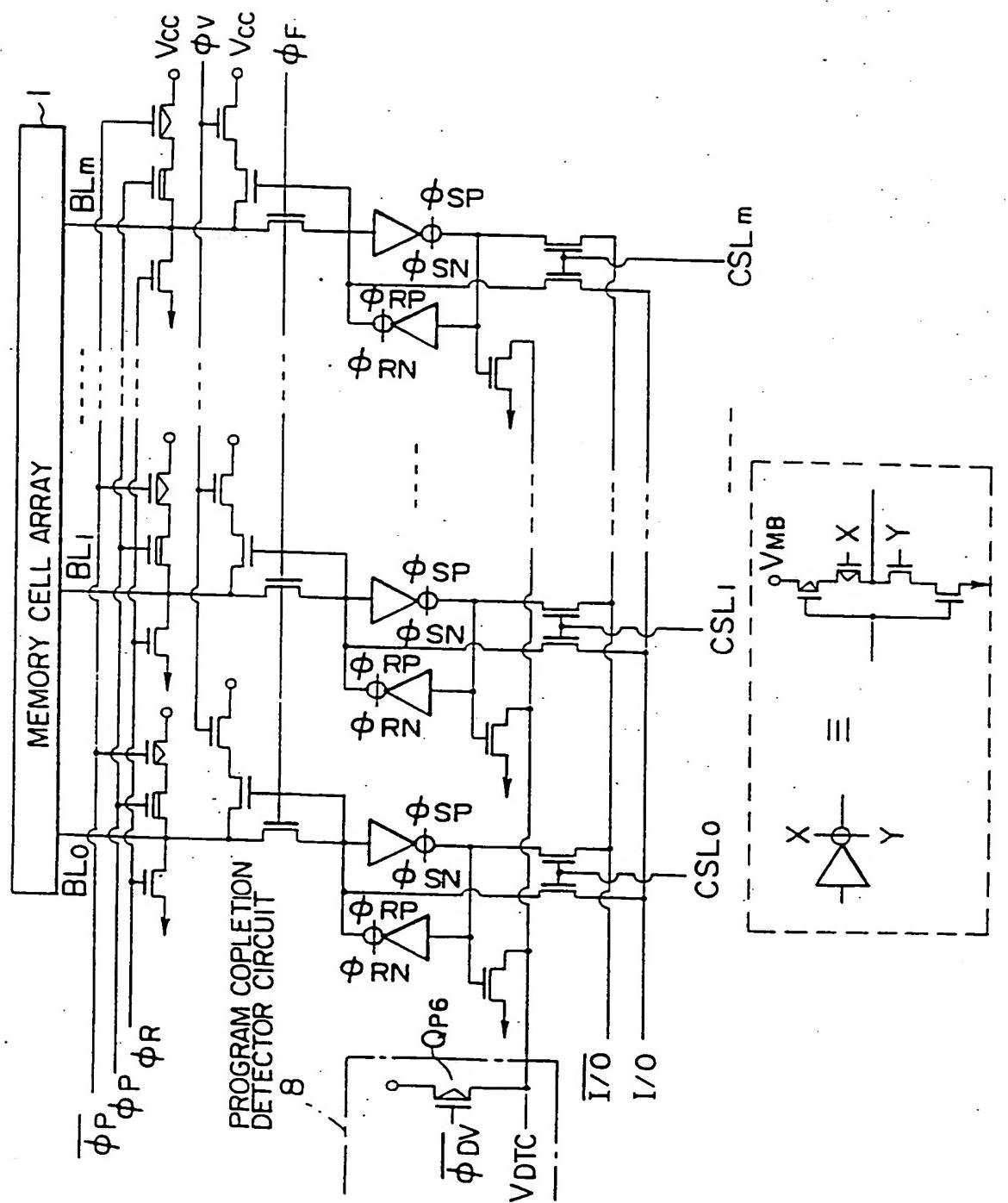


FIG. 6

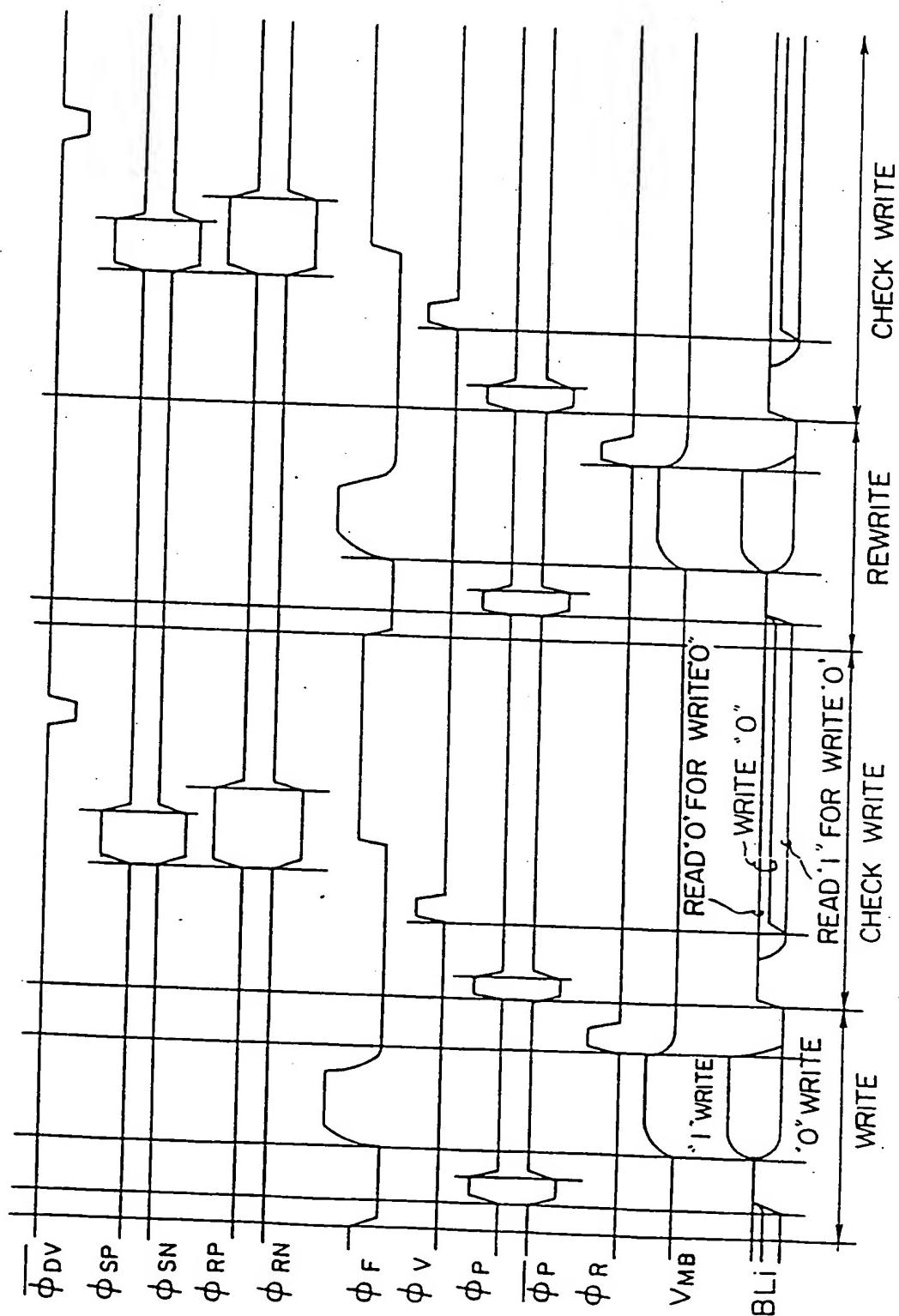


FIG. 7

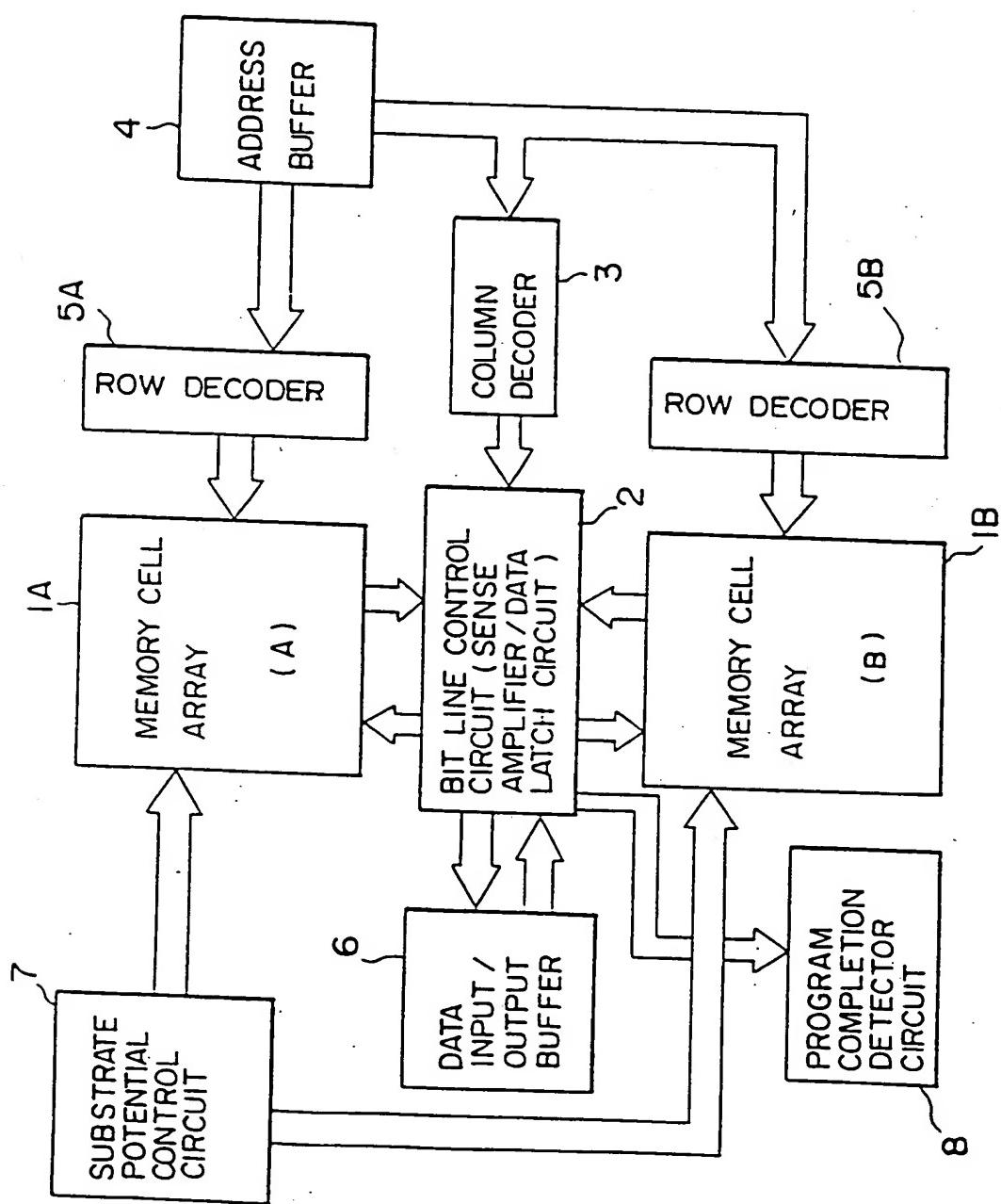


FIG. 8

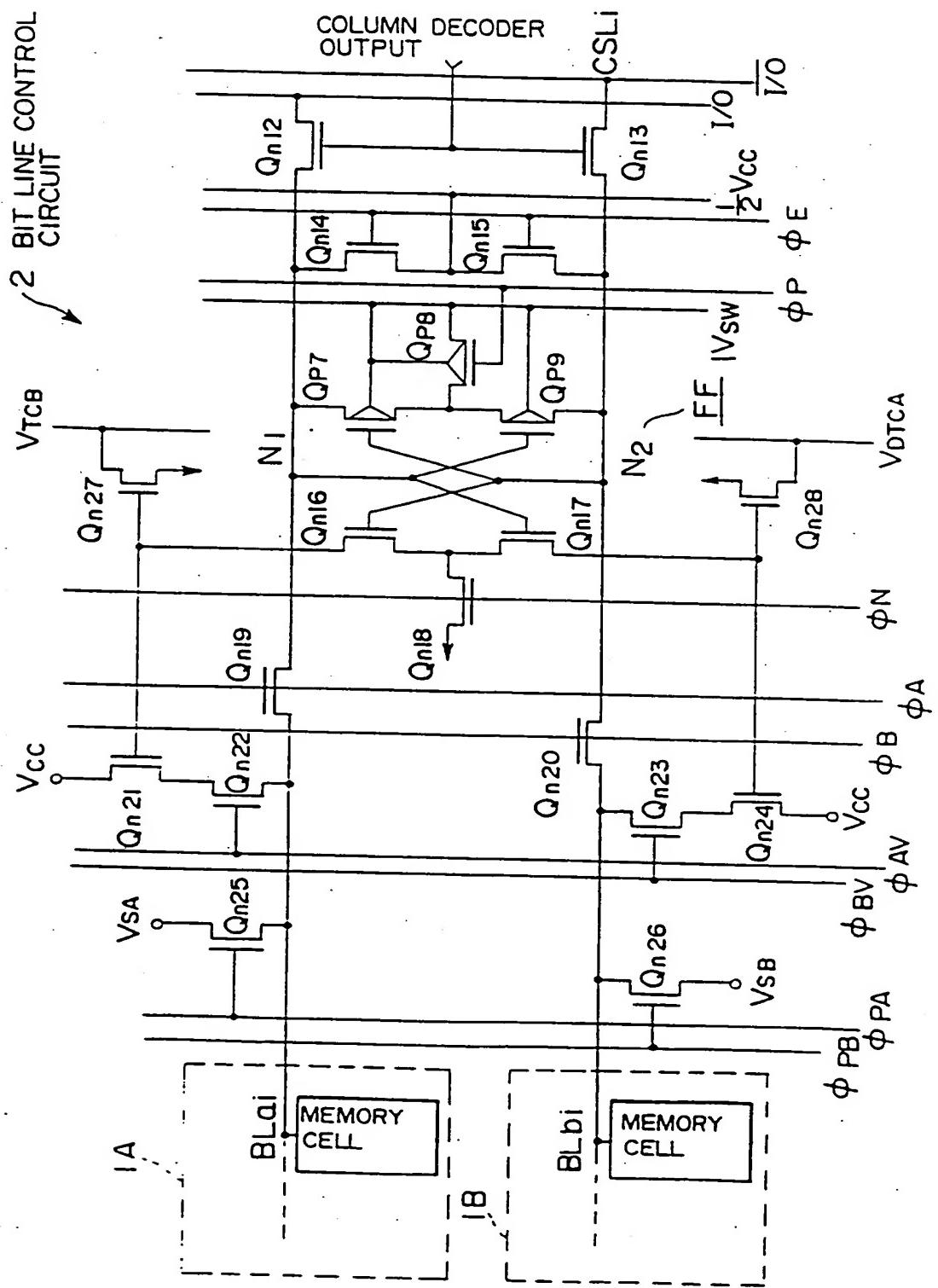


FIG. 9

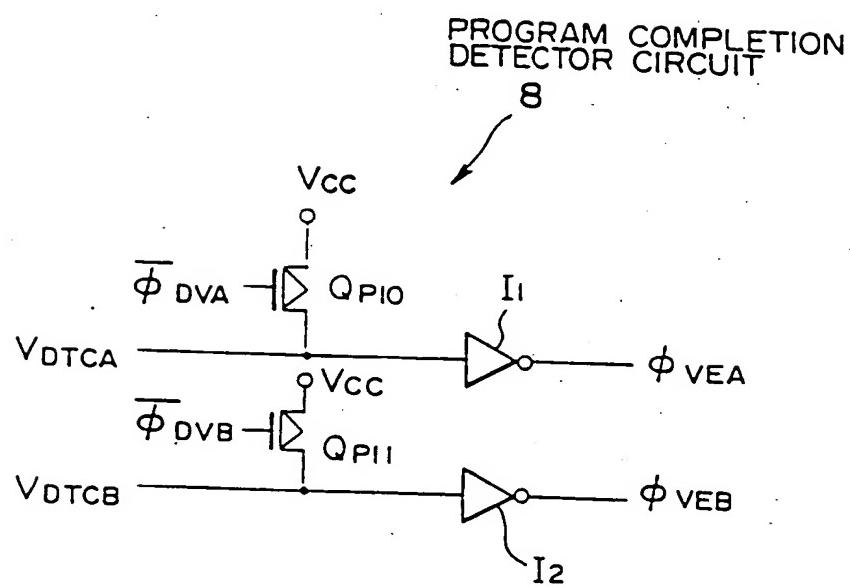


FIG.10

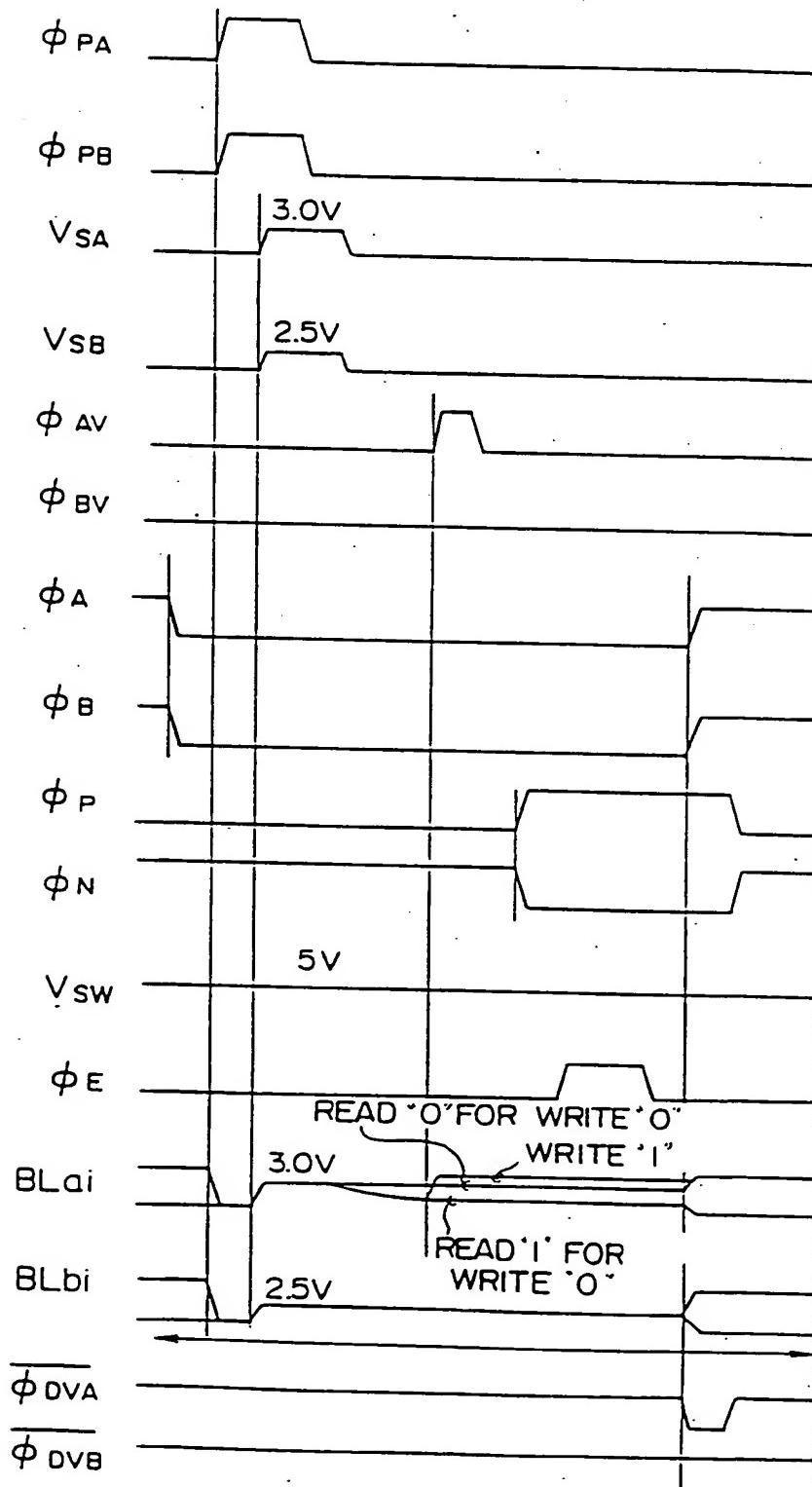


FIG. II

FIG. 12(a)

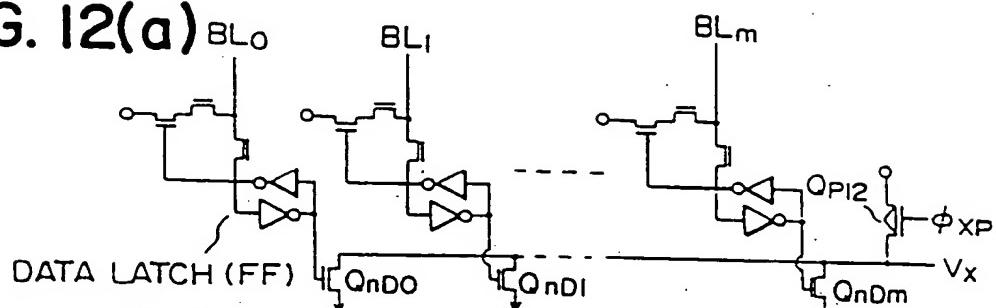


FIG. 12(b)

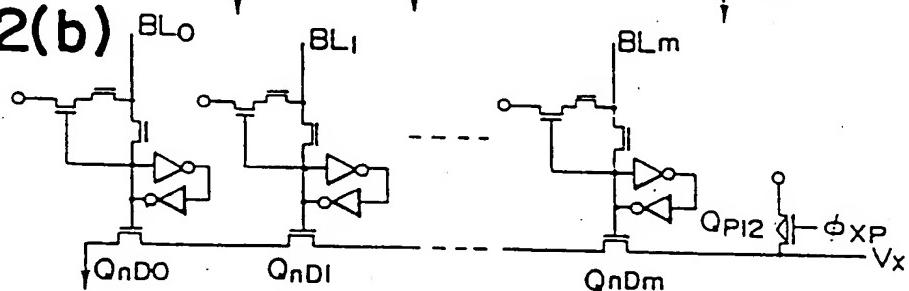


FIG. 12(c)

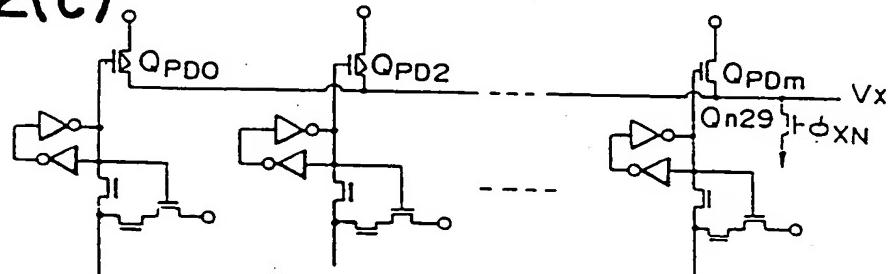


FIG. 12(d)

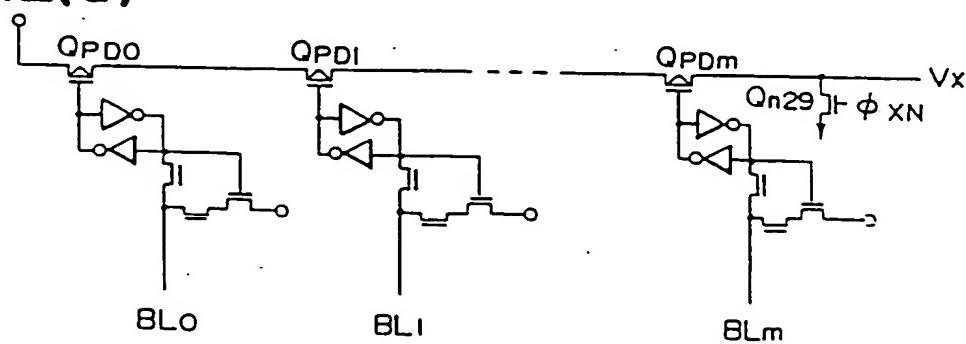


FIG. 13(a)

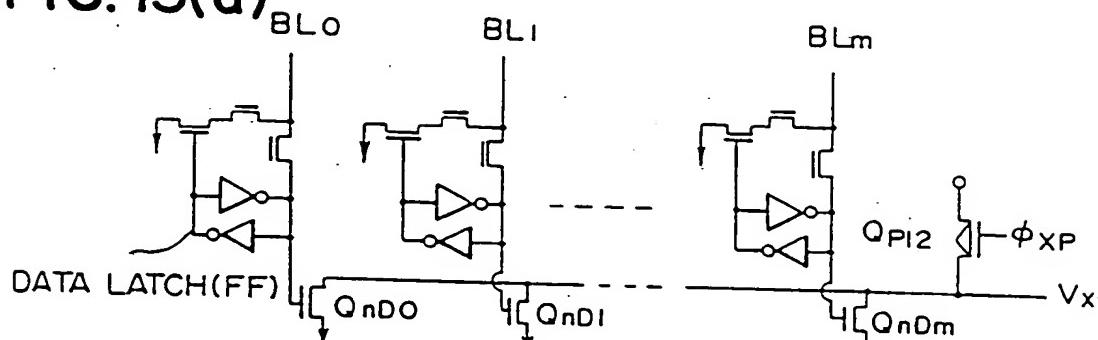


FIG. 13(b)

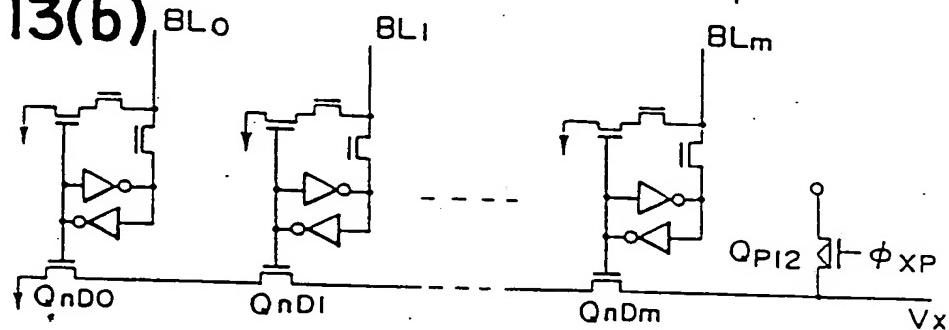


FIG. 13(c)

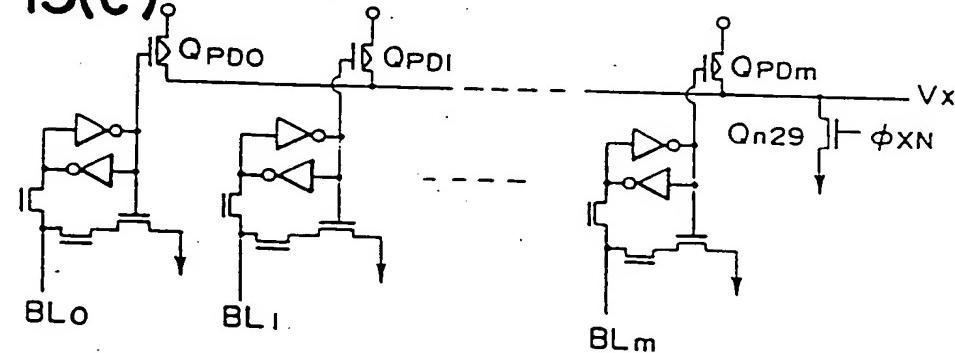
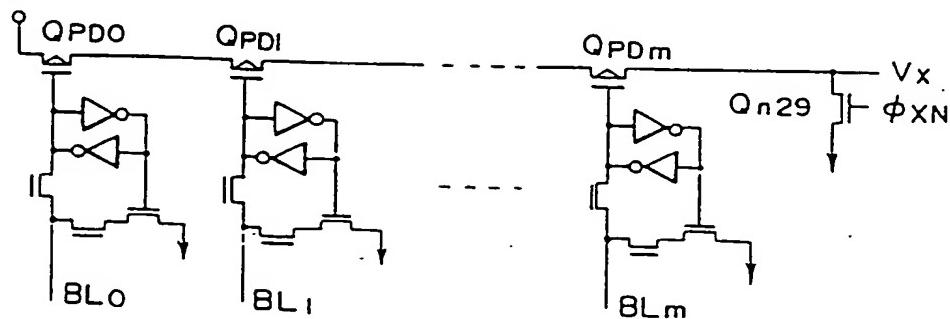


FIG. 13(d)



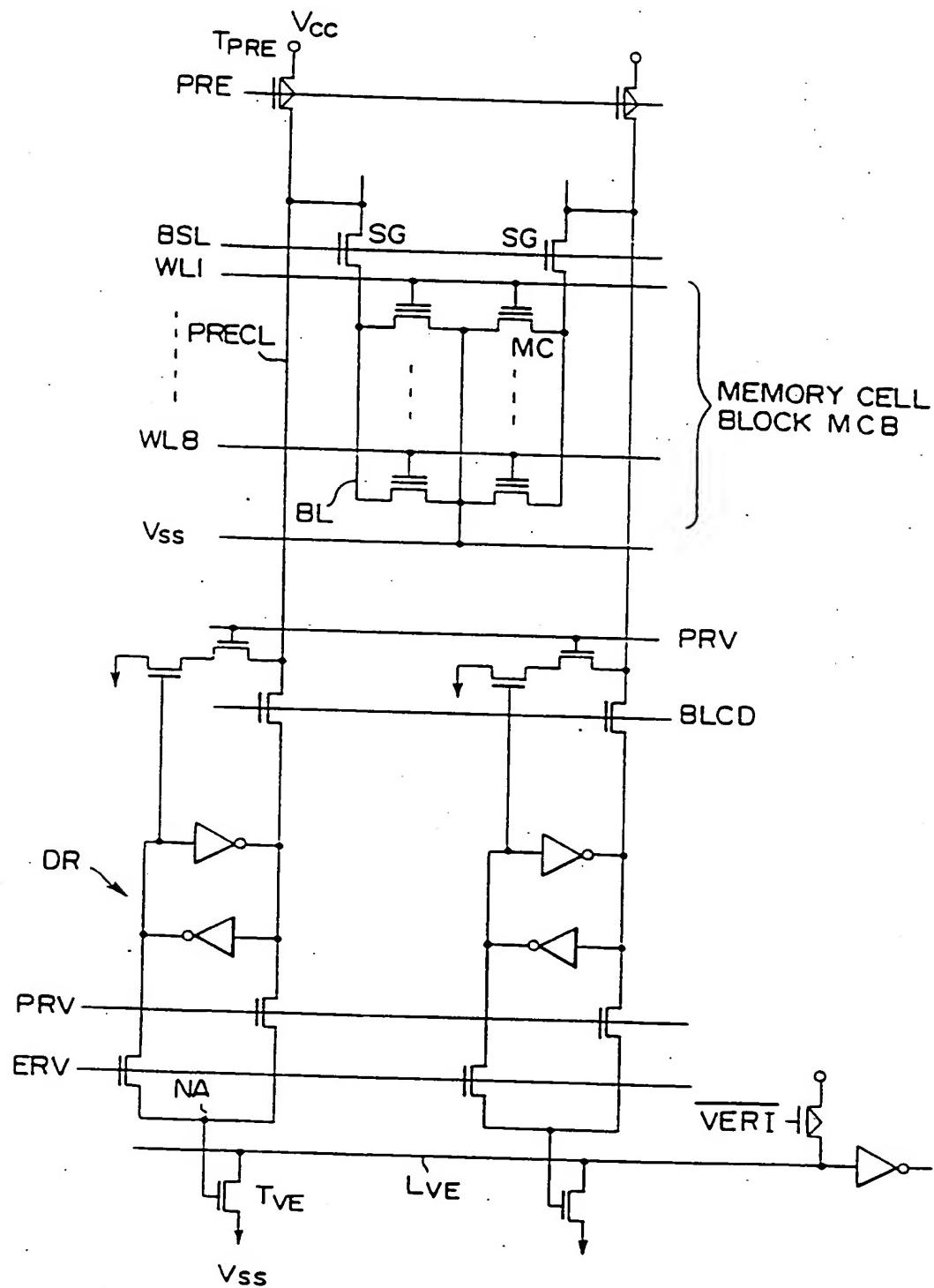


FIG. 14

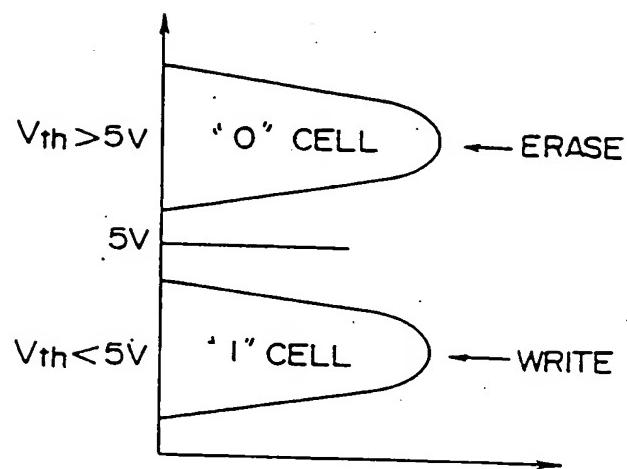
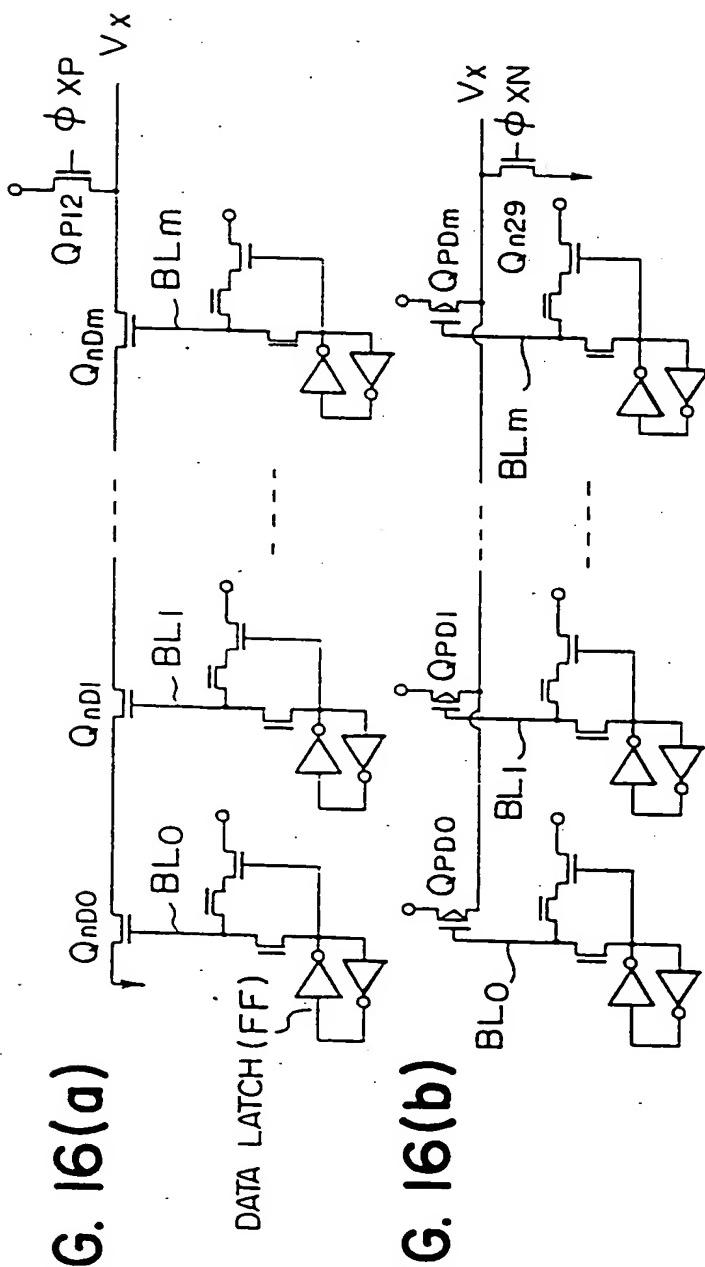


FIG. 15



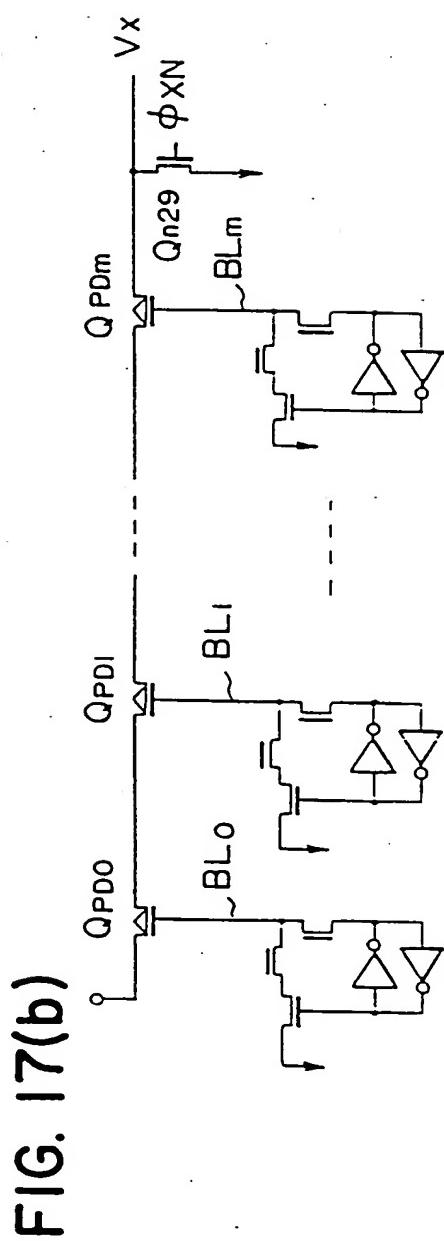
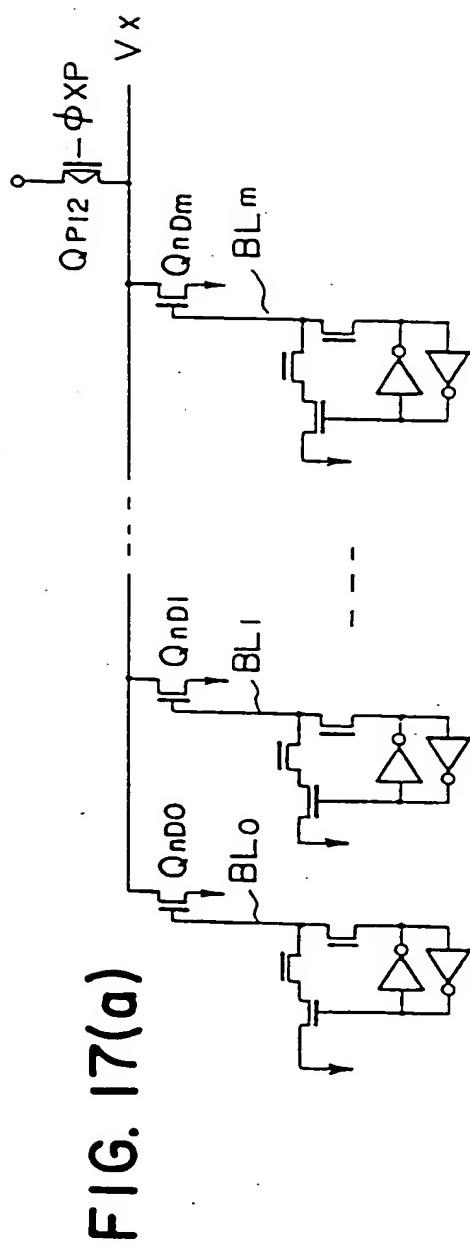


FIG. 18(a)

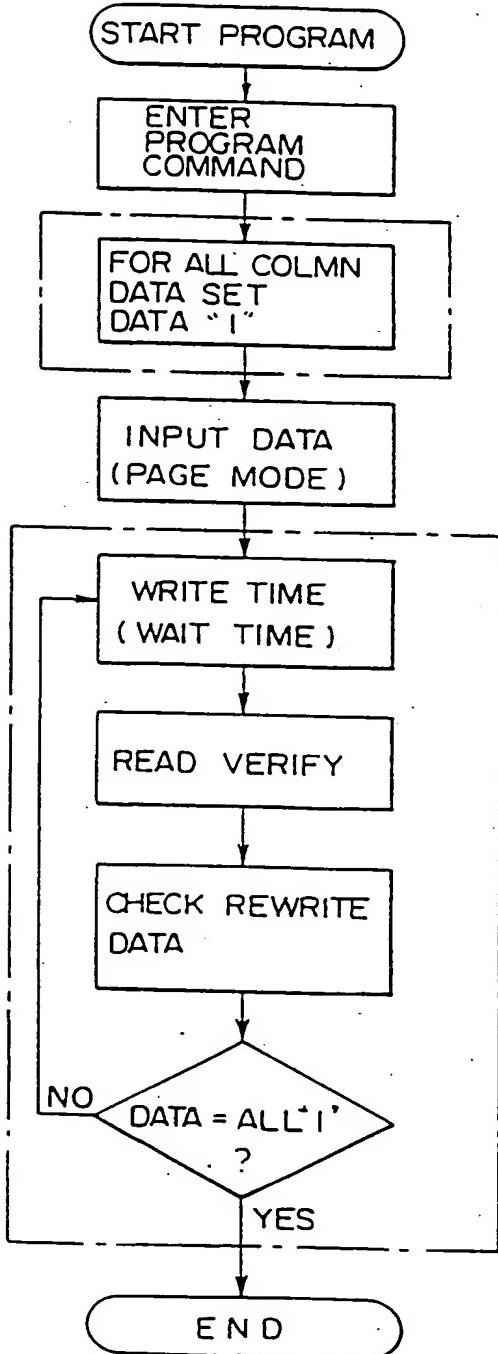


FIG. 18(b)

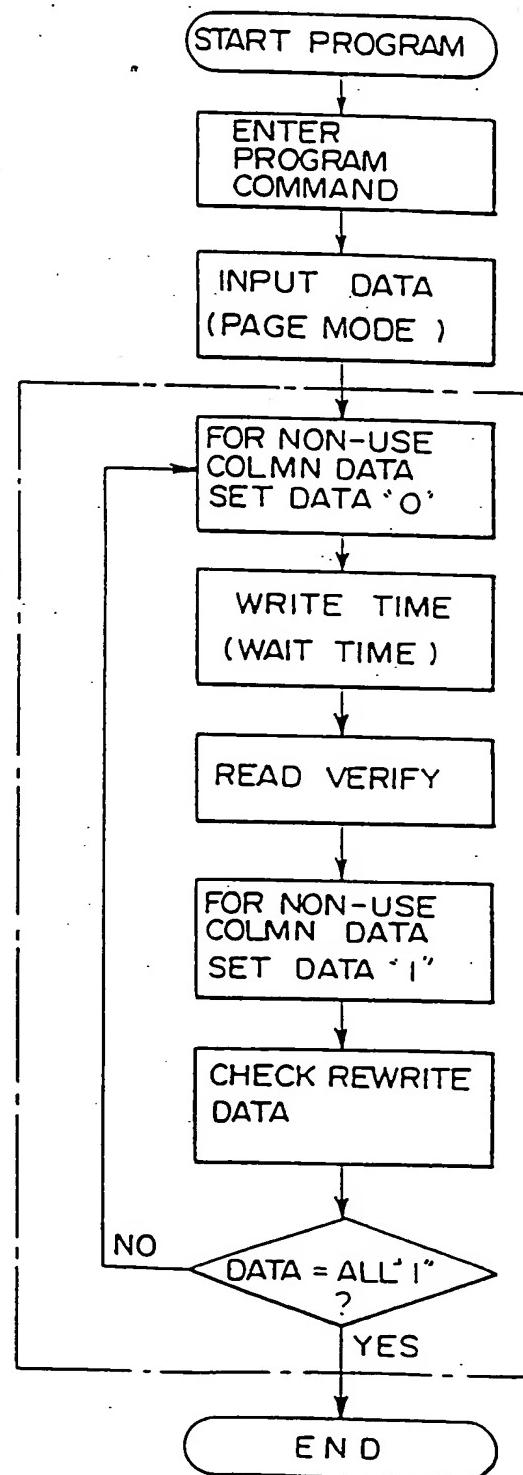


FIG. 19(a)

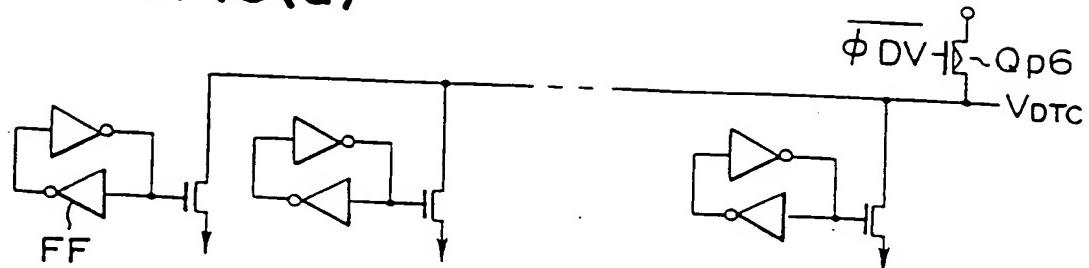


FIG. 19(b)

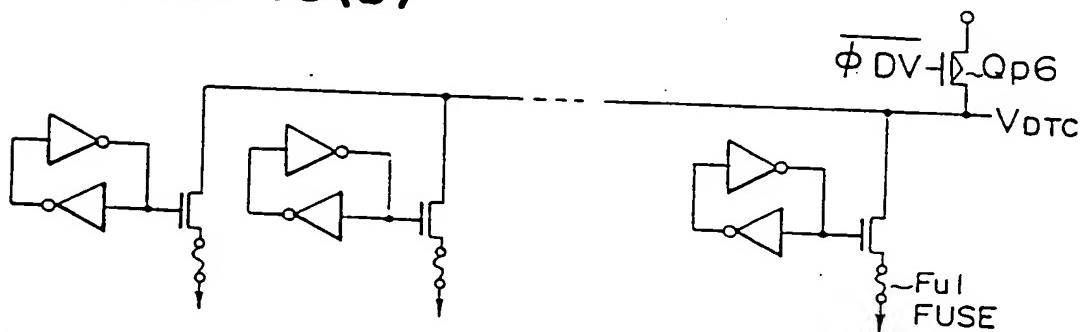


FIG. 19(c)

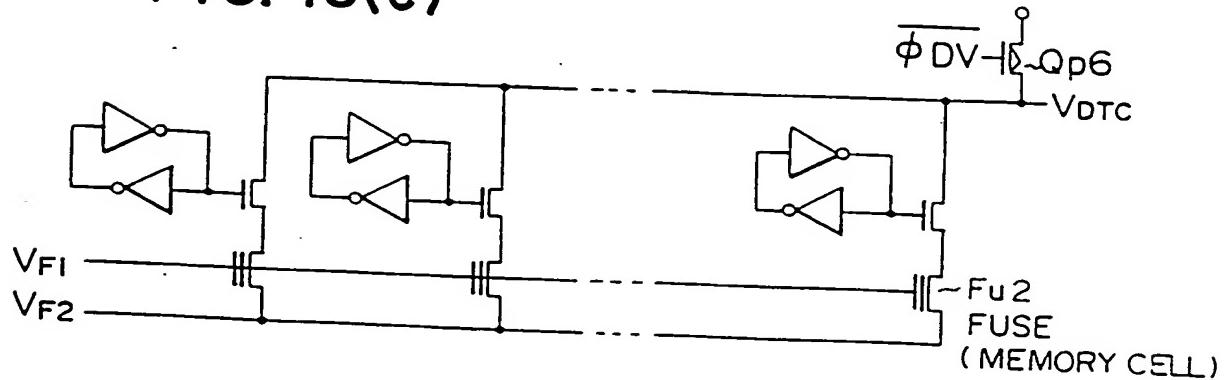


FIG. 20(b)

FIG. 20(a)

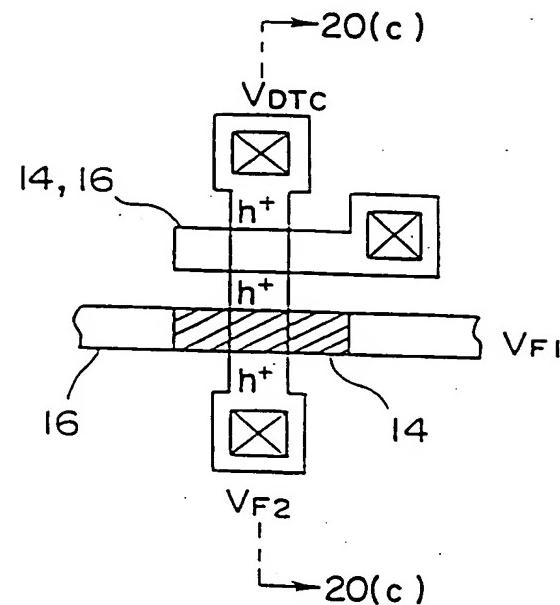
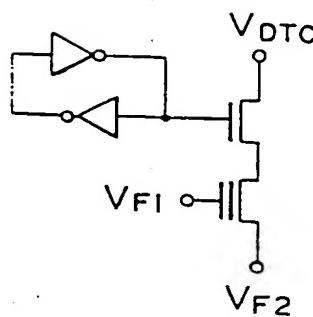


FIG. 20(c)

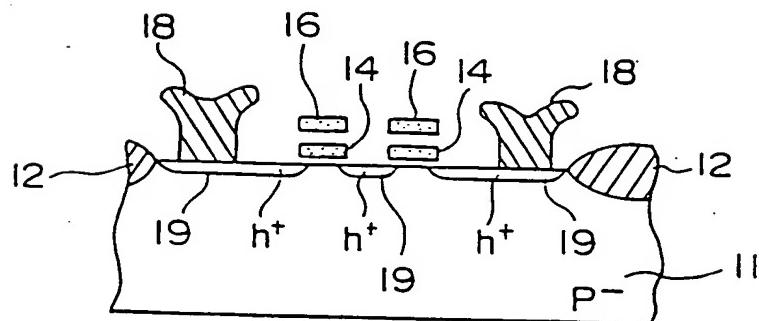


FIG. 2I(a)

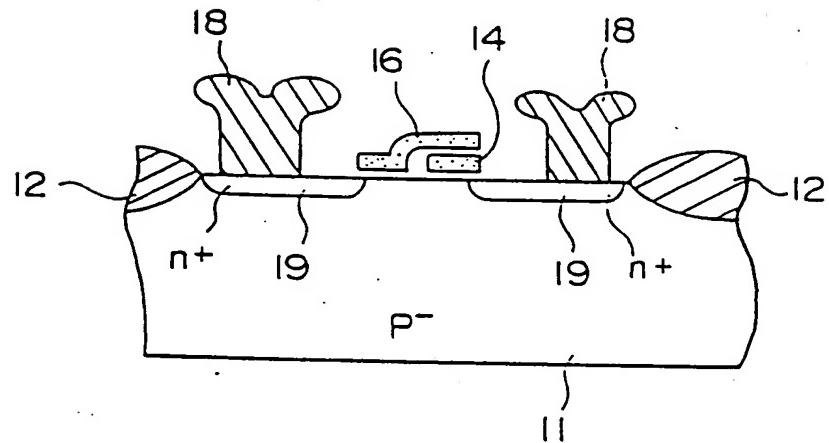


FIG. 2I(b)

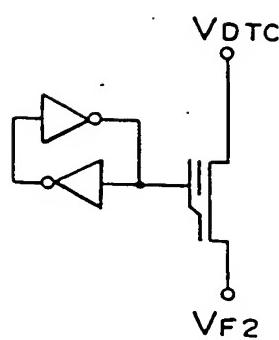
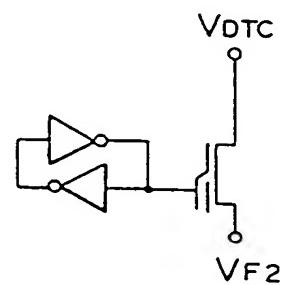


FIG. 2I(c)



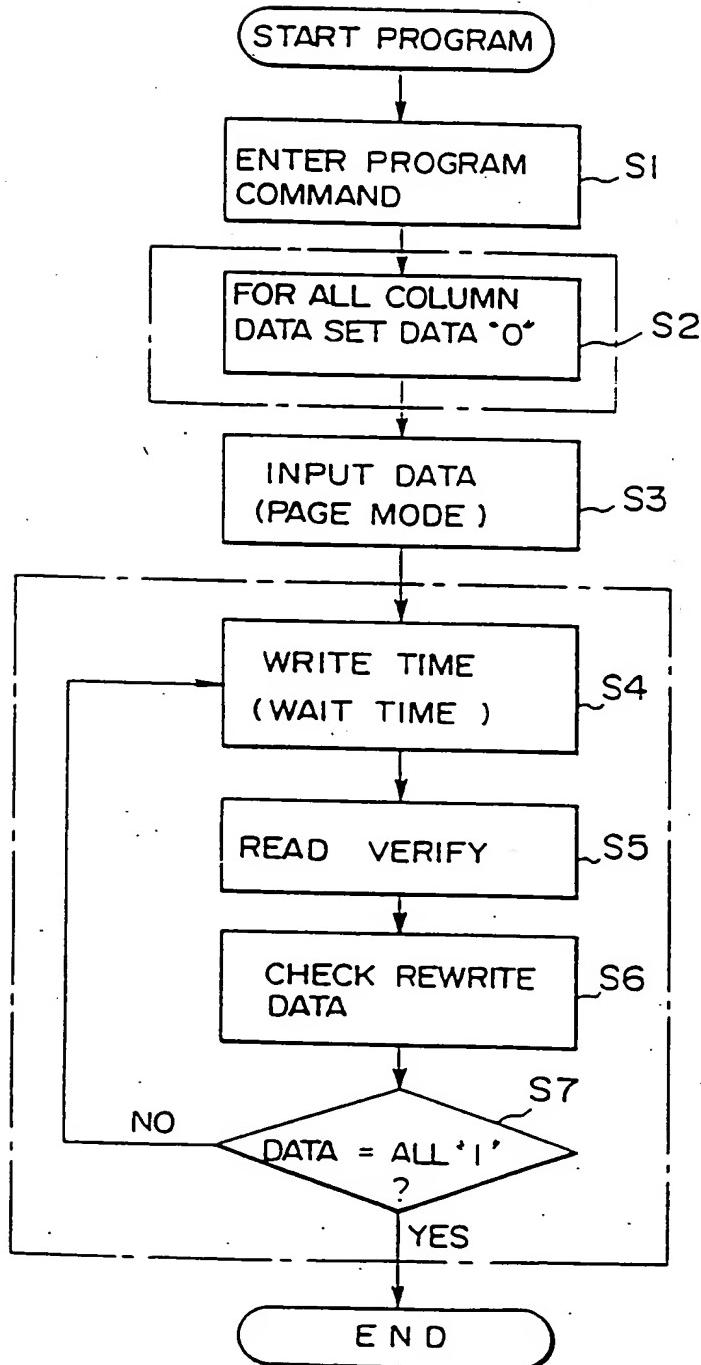


FIG. 22

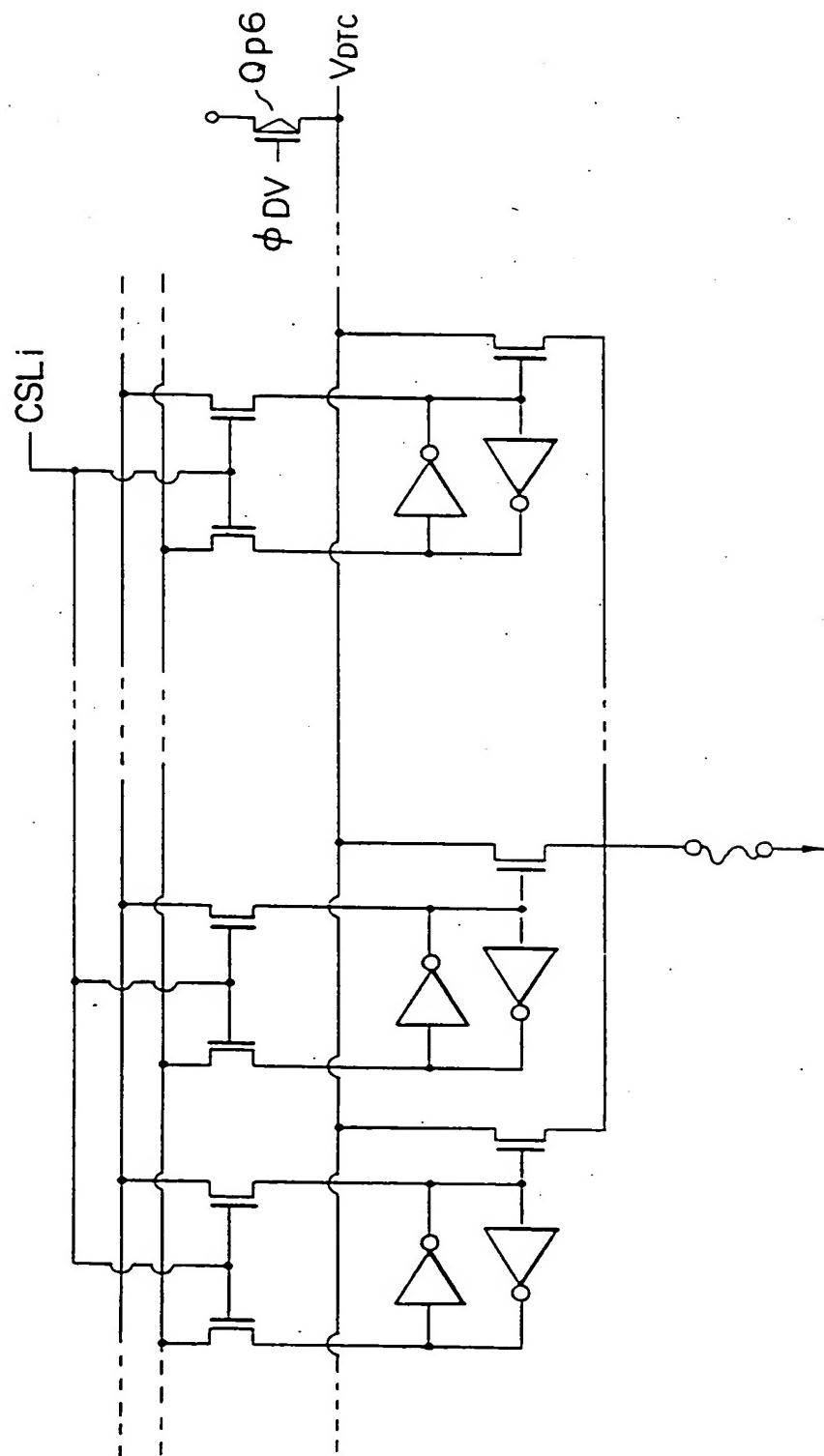


FIG. 23

FIG. 24(a)

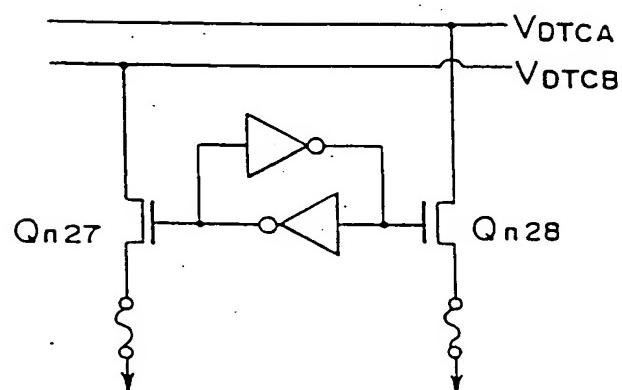


FIG. 24(b)

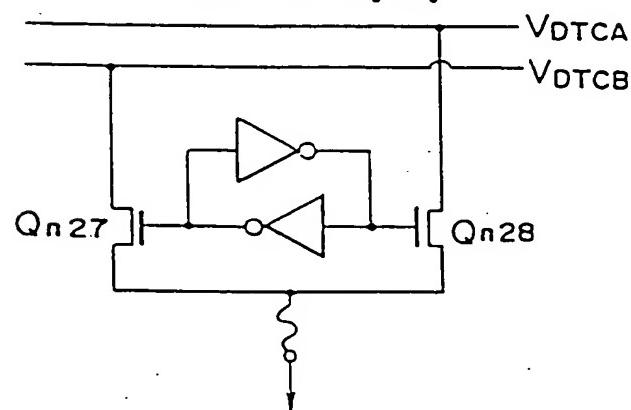


FIG. 25(a)

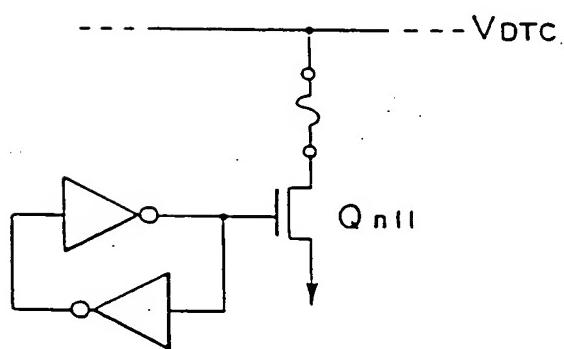


FIG. 25(b)

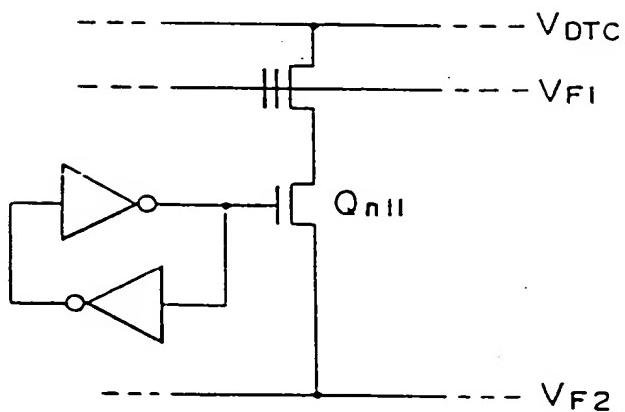


FIG. 26(a)

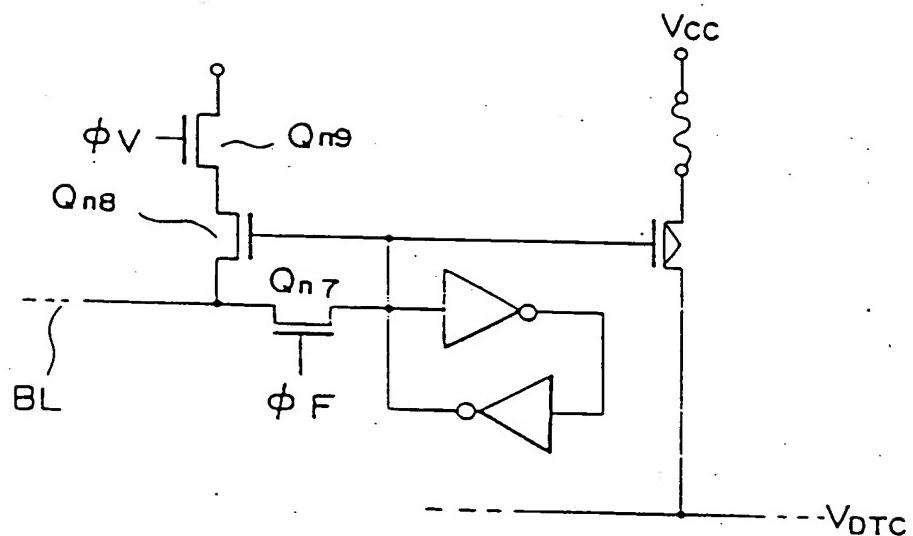


FIG. 26(b)

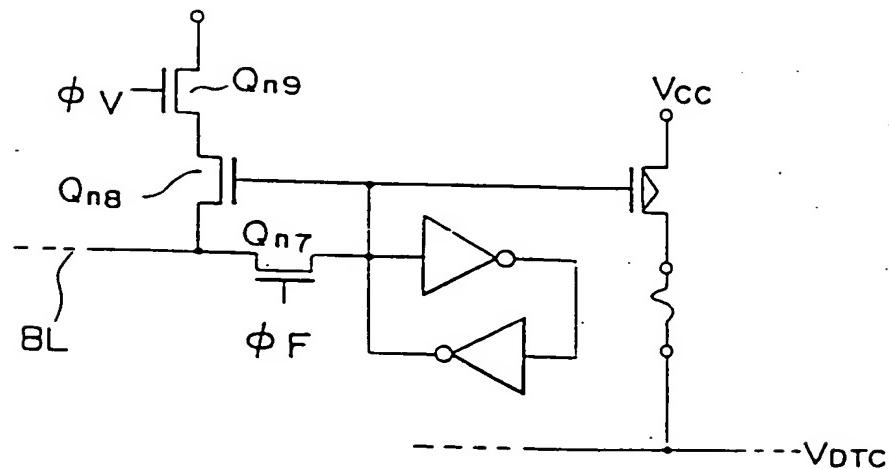


FIG. 27(a)

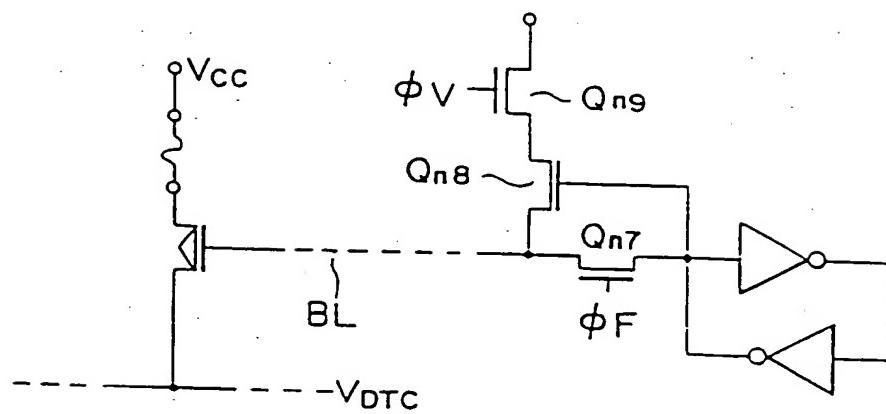


FIG. 27(b)

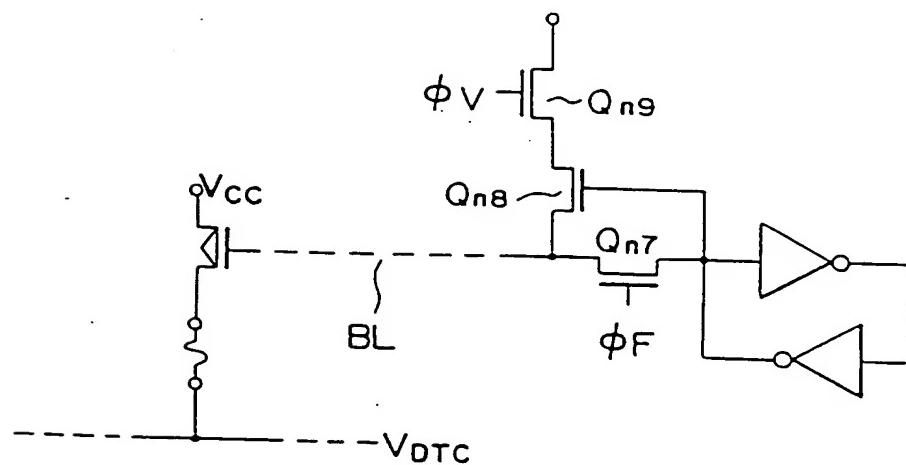


FIG. 28(a)

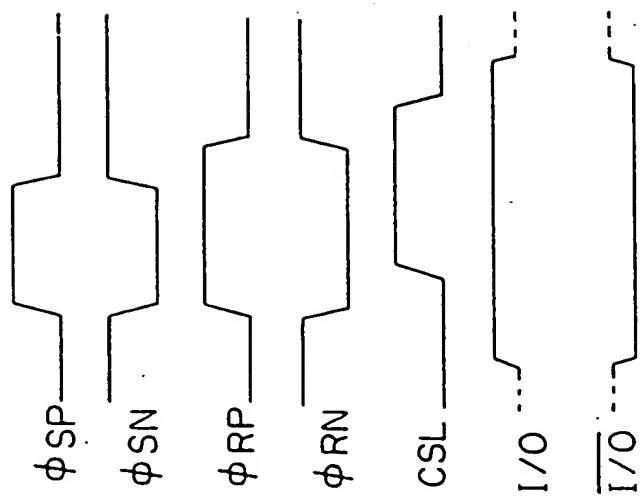
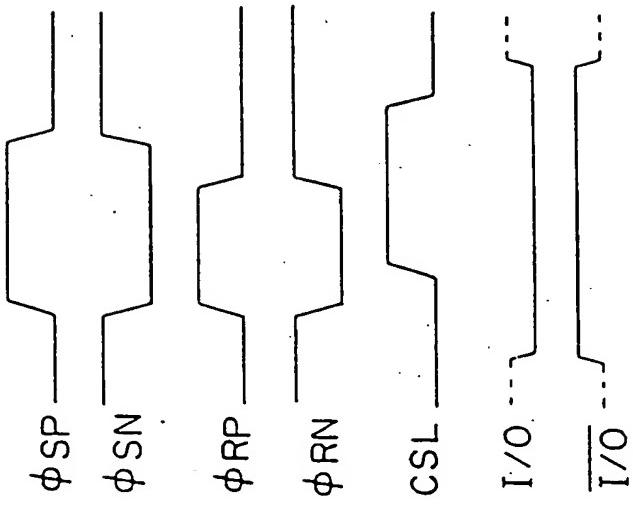


FIG. 28(b)



Title: NON-VOLATILE SEMICONDUCTOR
MEMORY DEVICE AND MEMORY
SYSTEM USING THE SAME
Inventor(s): Tomoharu TANAKA et al.
DOCKET NO.: 016887-1102

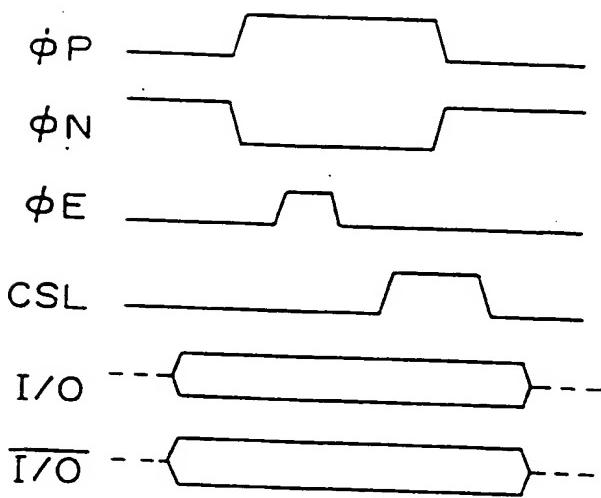


FIG. 29

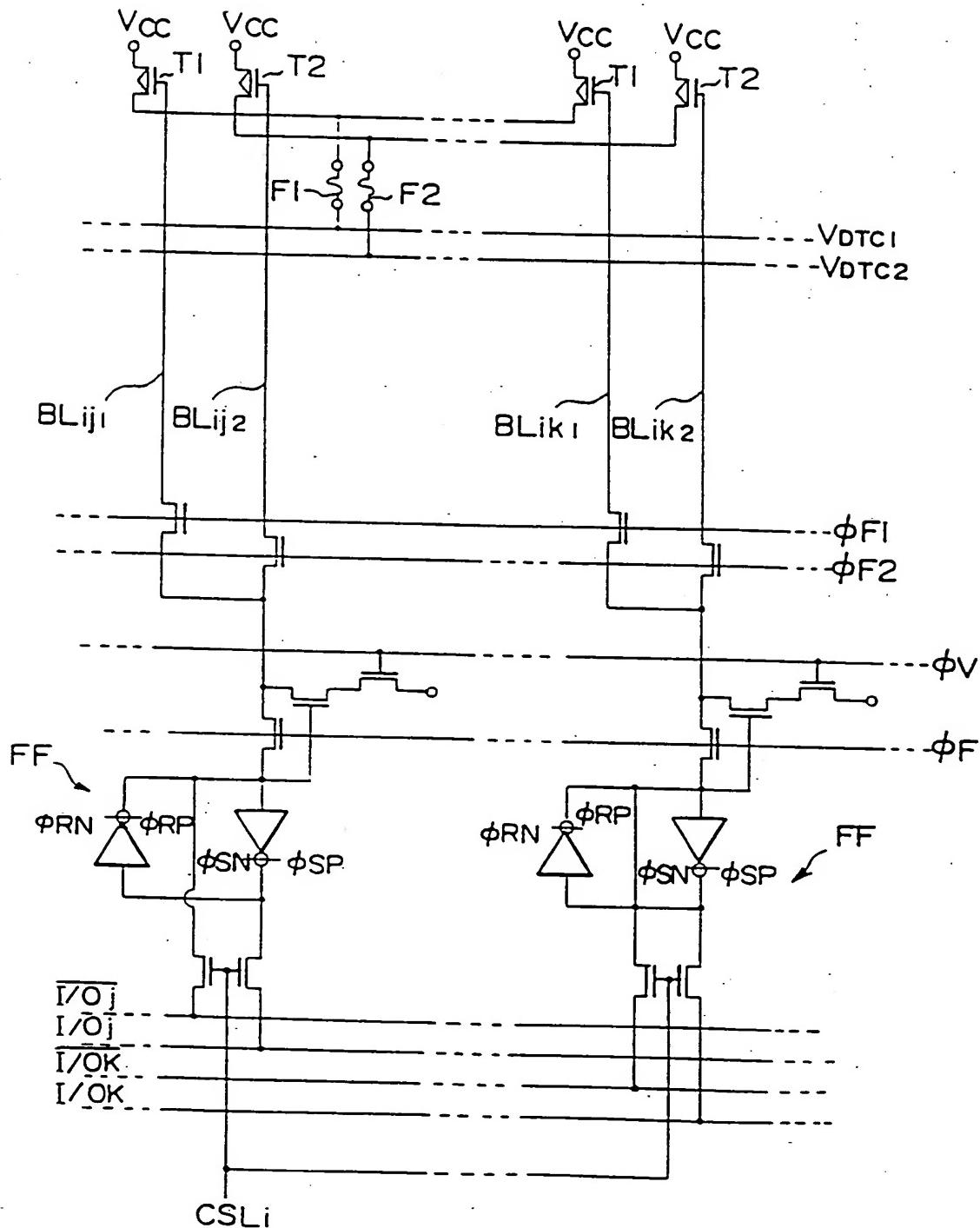


FIG. 30

FIG. 31(a)

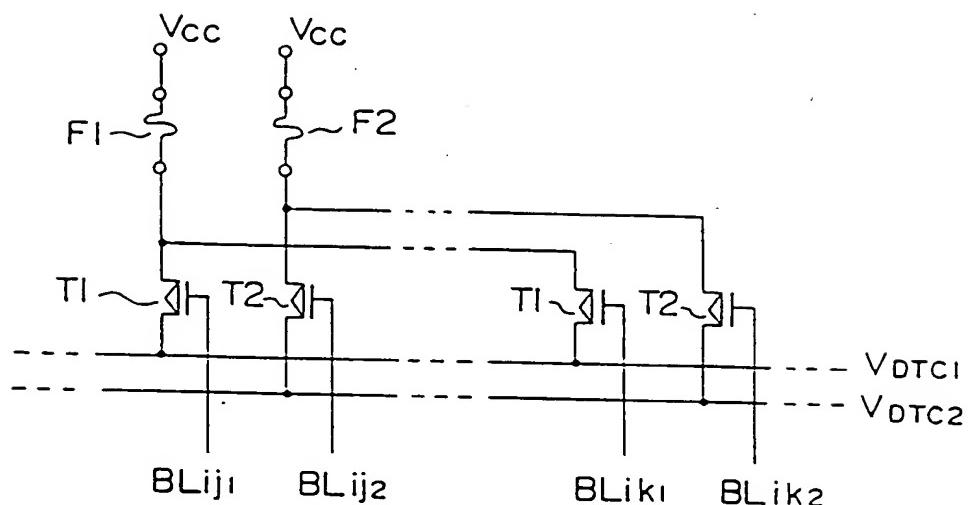
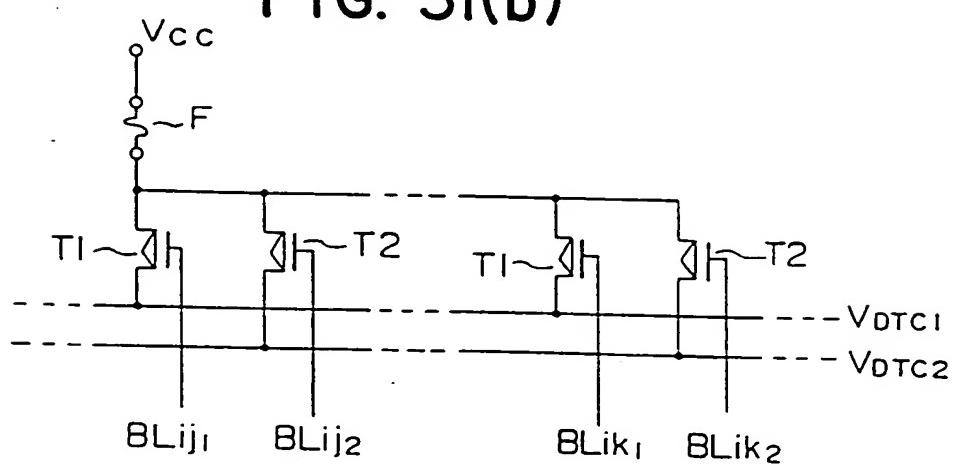


FIG. 3I(b)



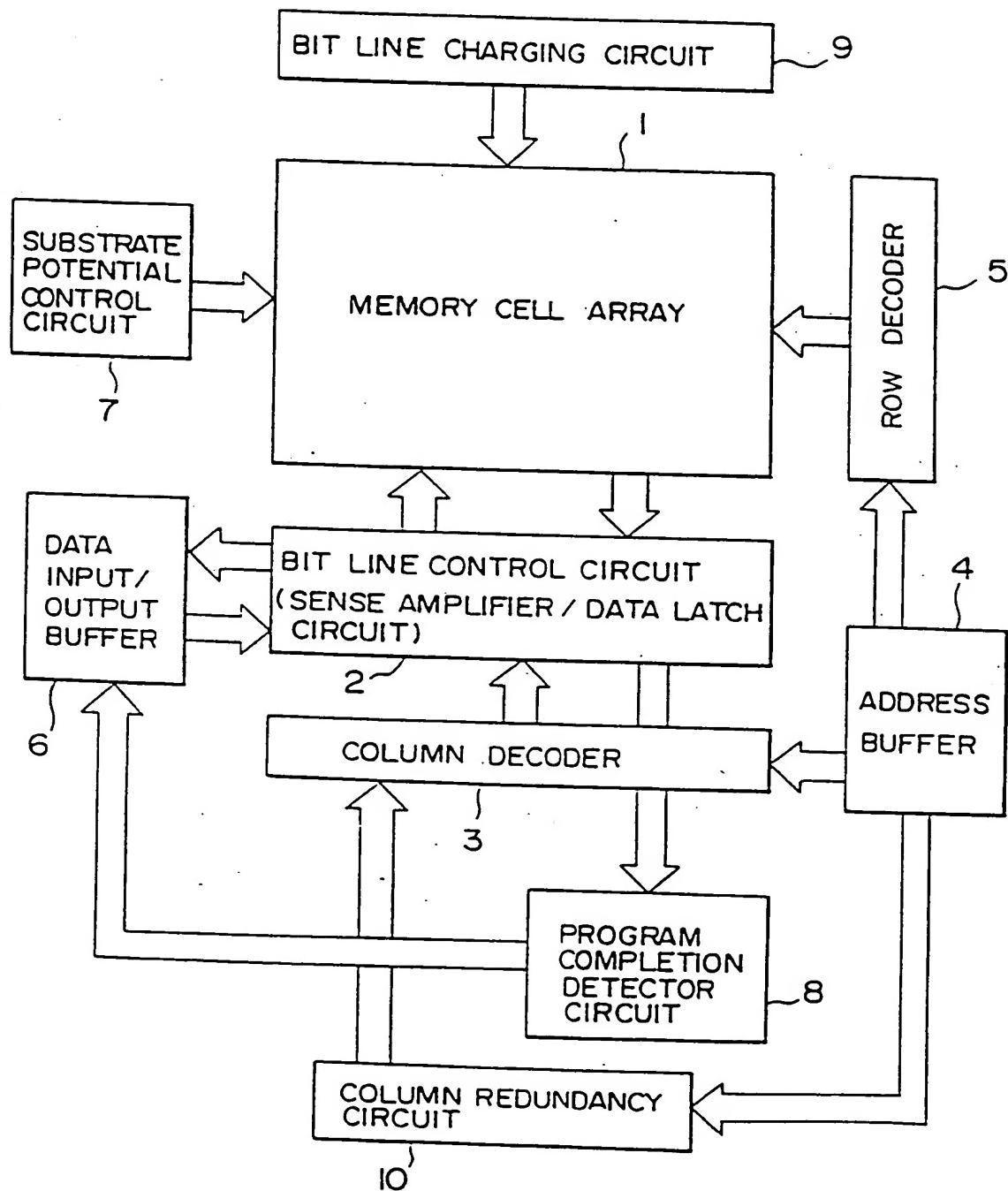


FIG. 32

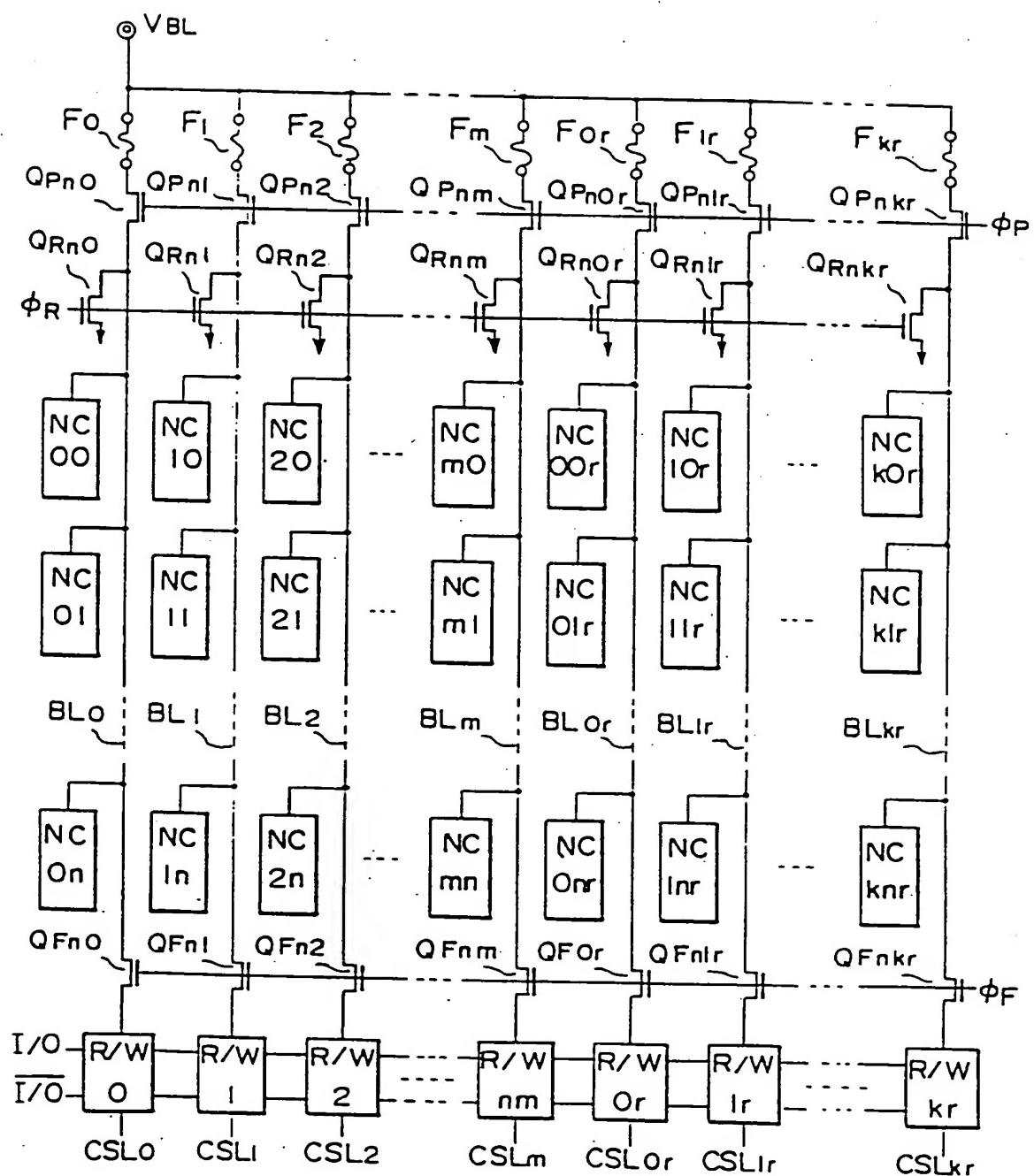


FIG. 33

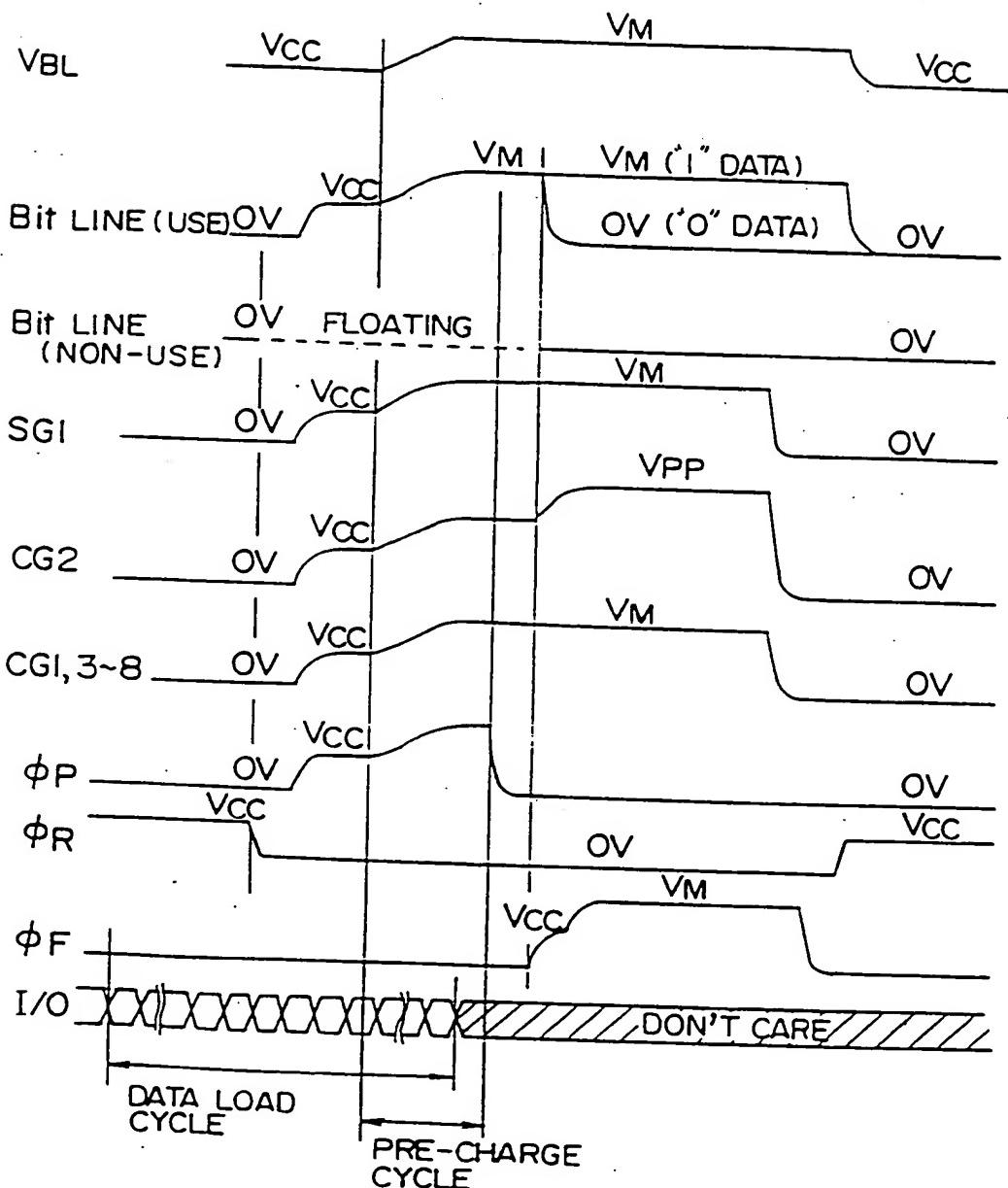


FIG.34

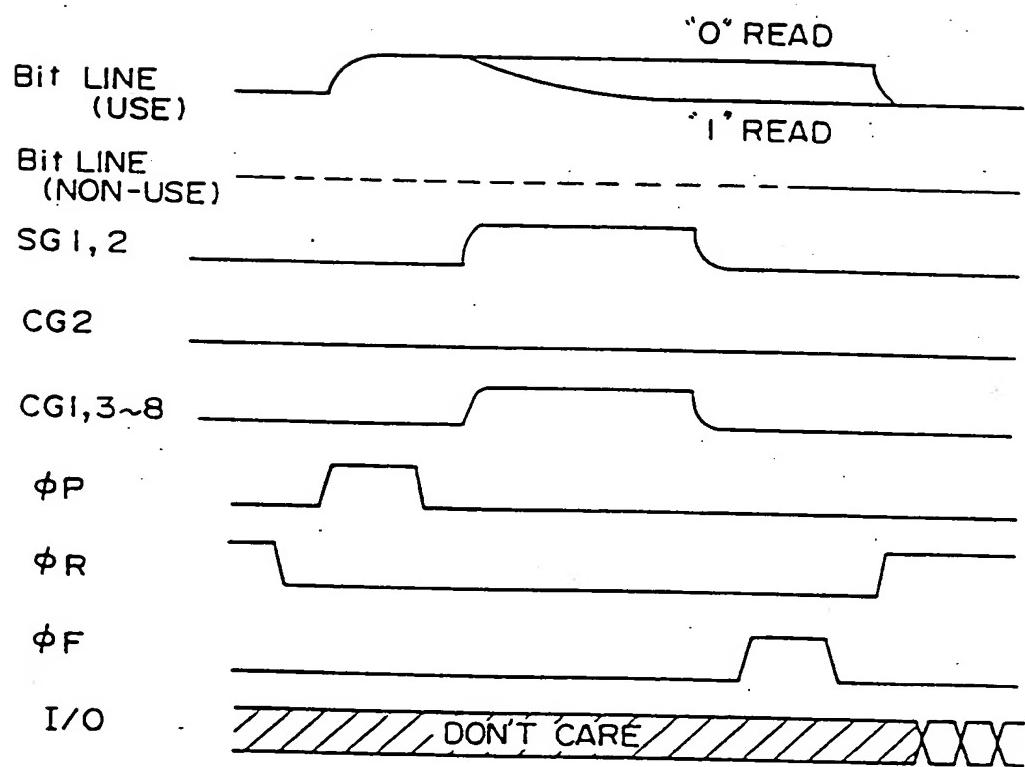


FIG.35

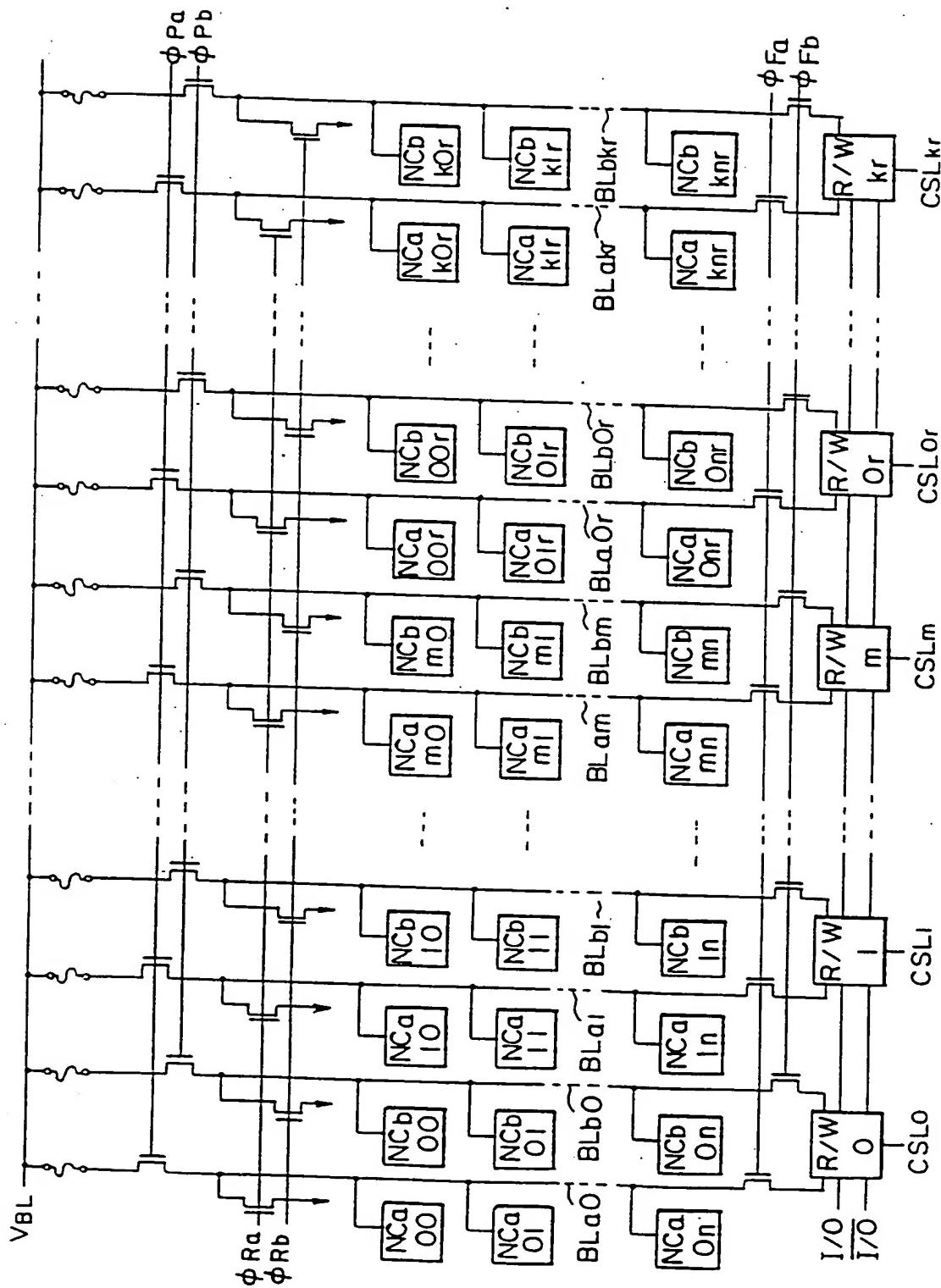


FIG. 36

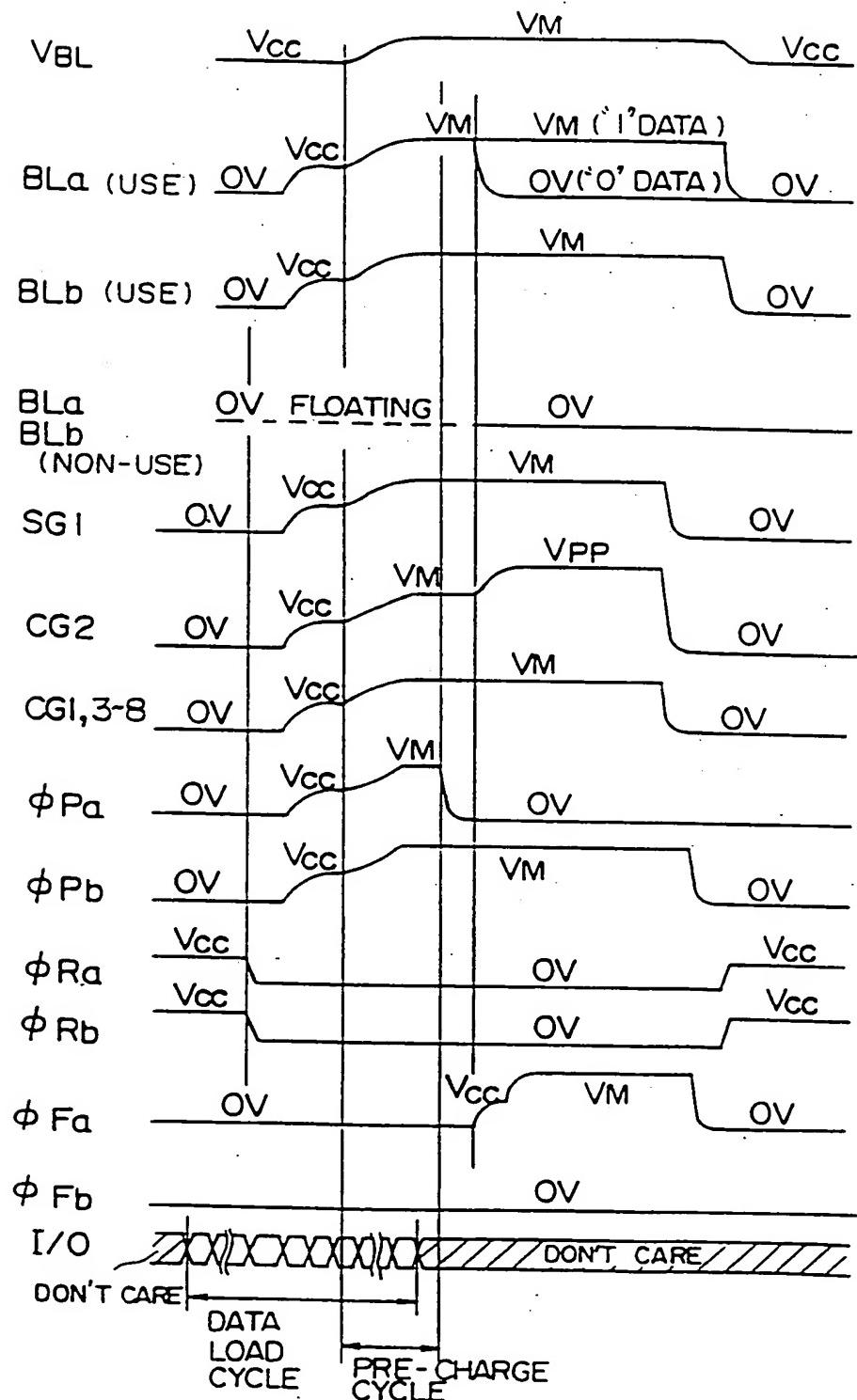


FIG.37

Title: NON-VOLATILE SEMICONDUCTOR
MEMORY DEVICE AND MEMORY
SYSTEM USING THE SAME
Inventor(s): Tomoharu TANAKA et al.
DOCKET NO.: 016887-1102

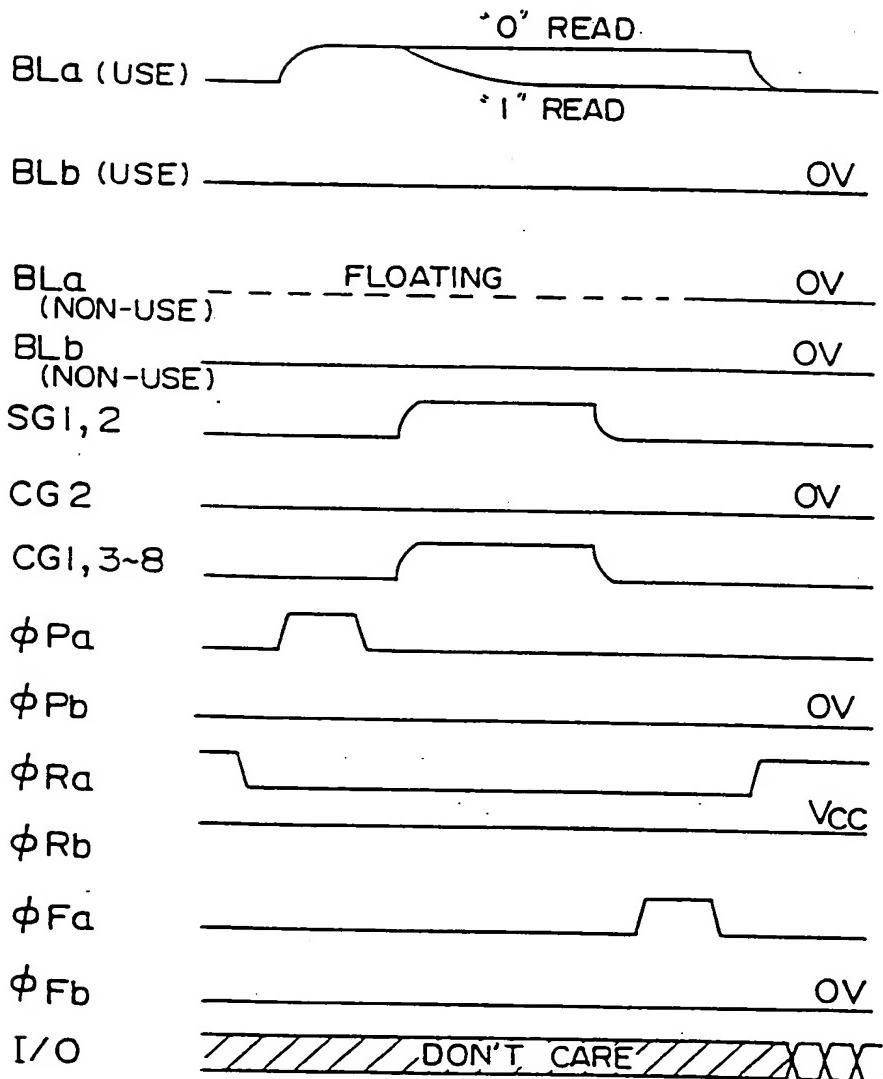


FIG. 38

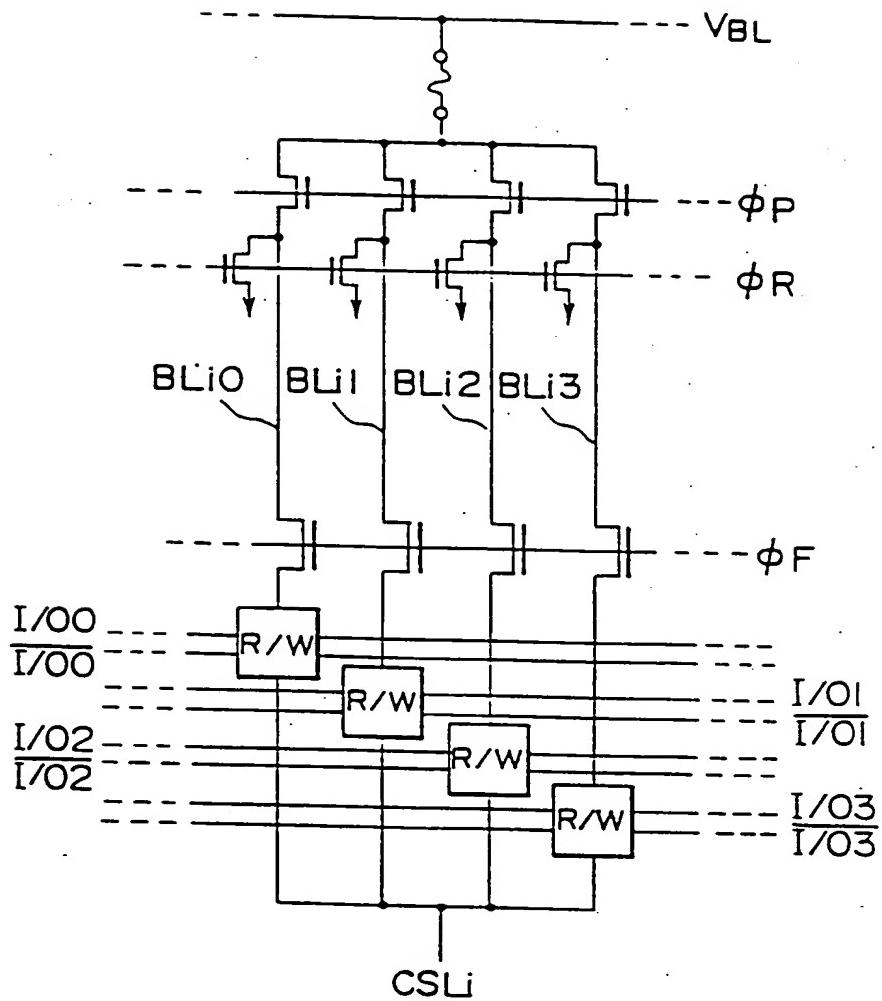


FIG.39

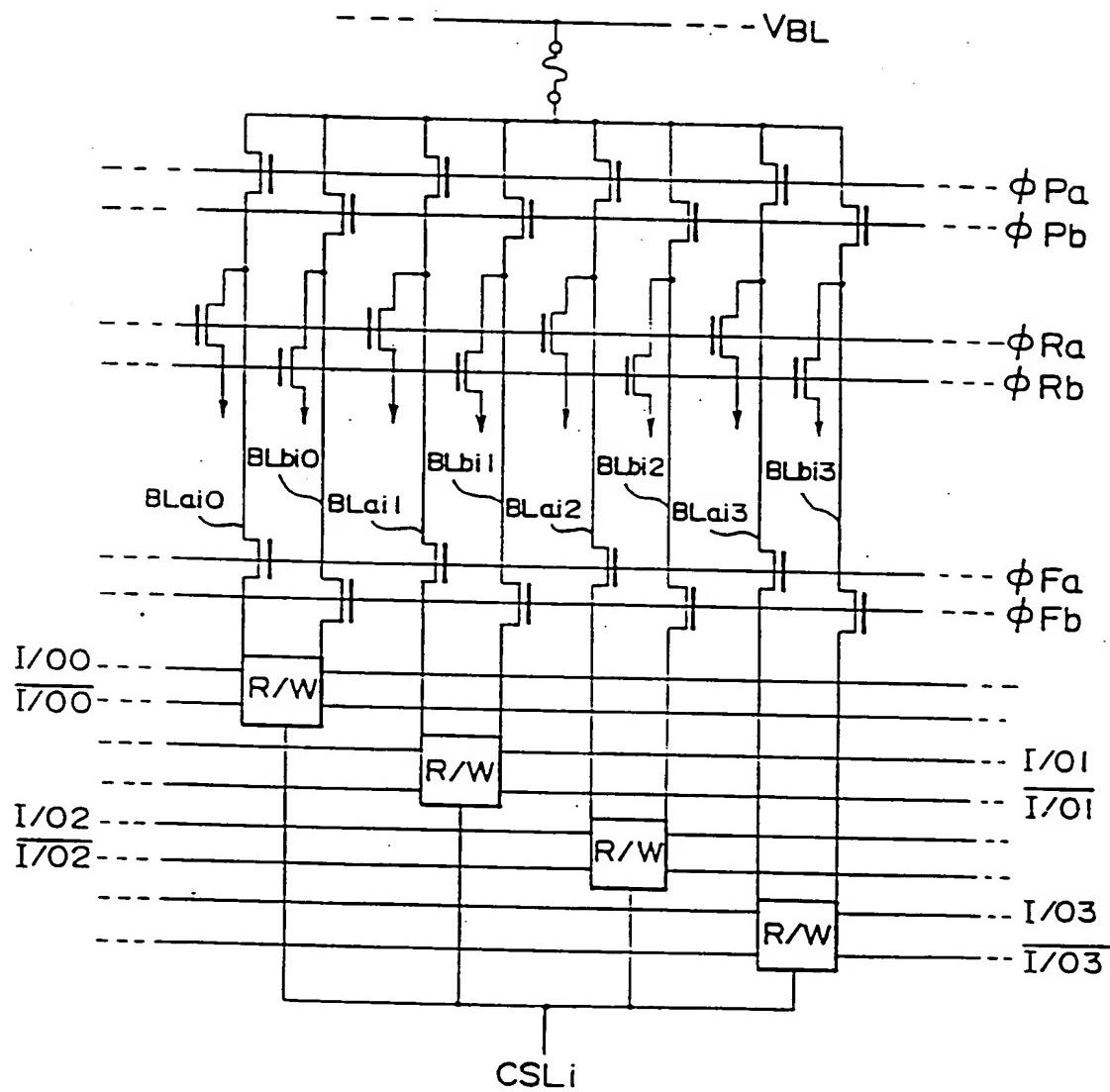


FIG. 40

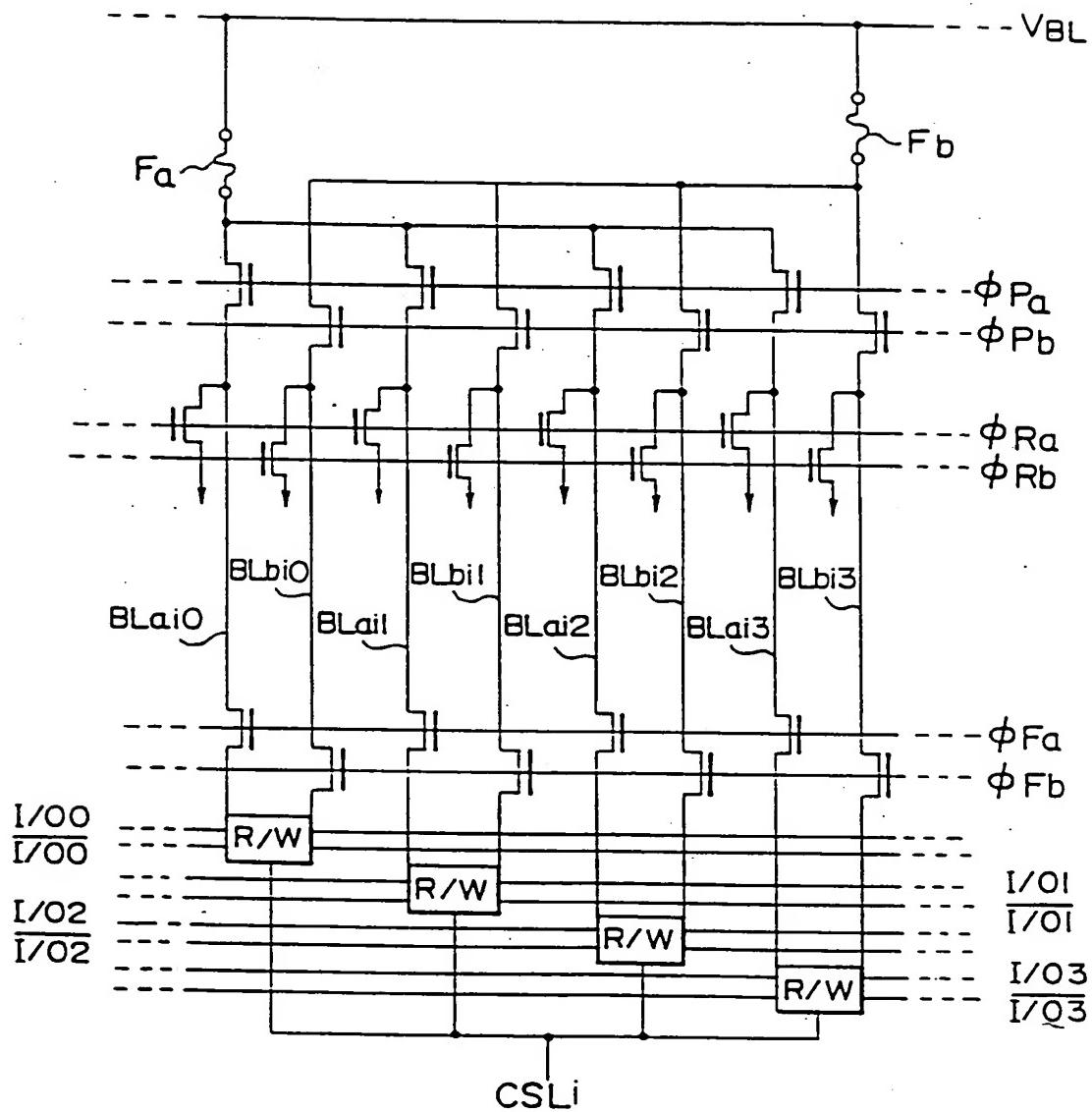
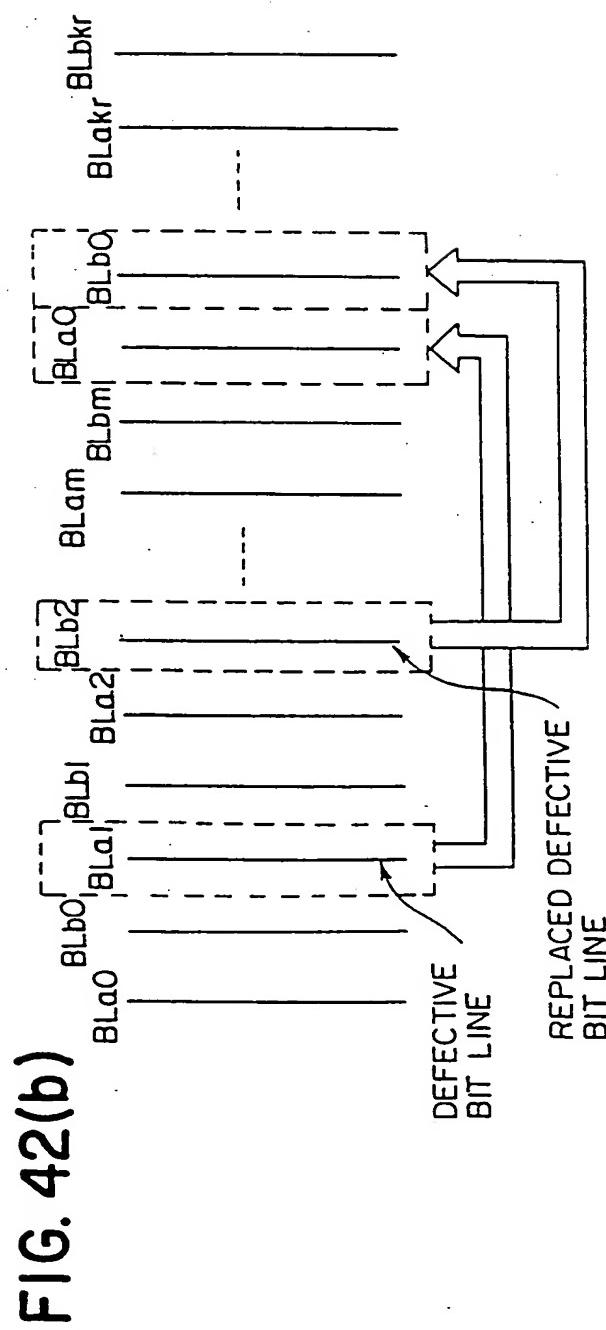
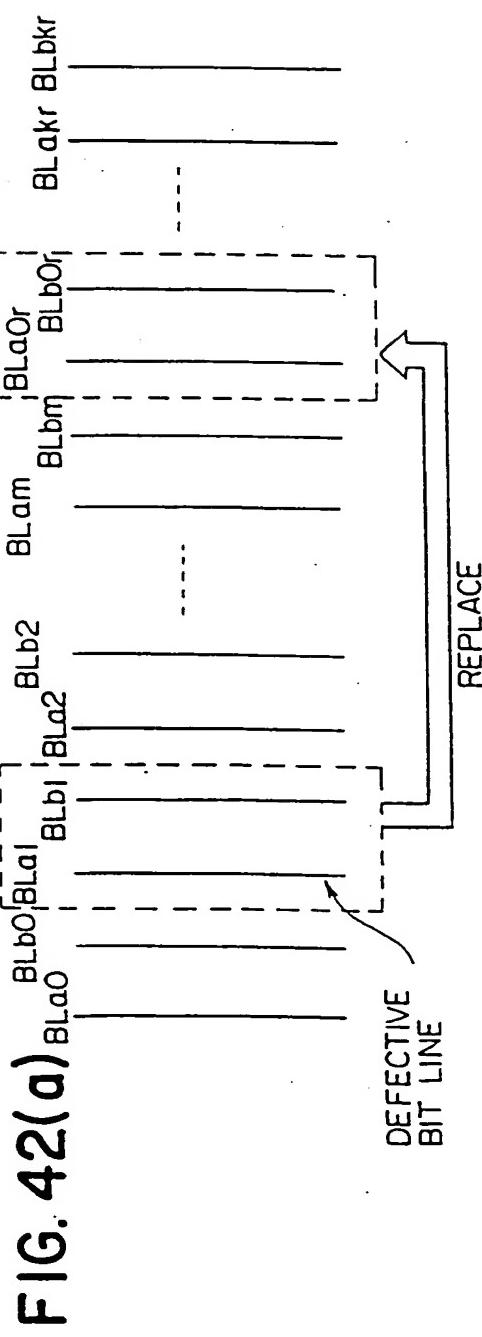


FIG. 41



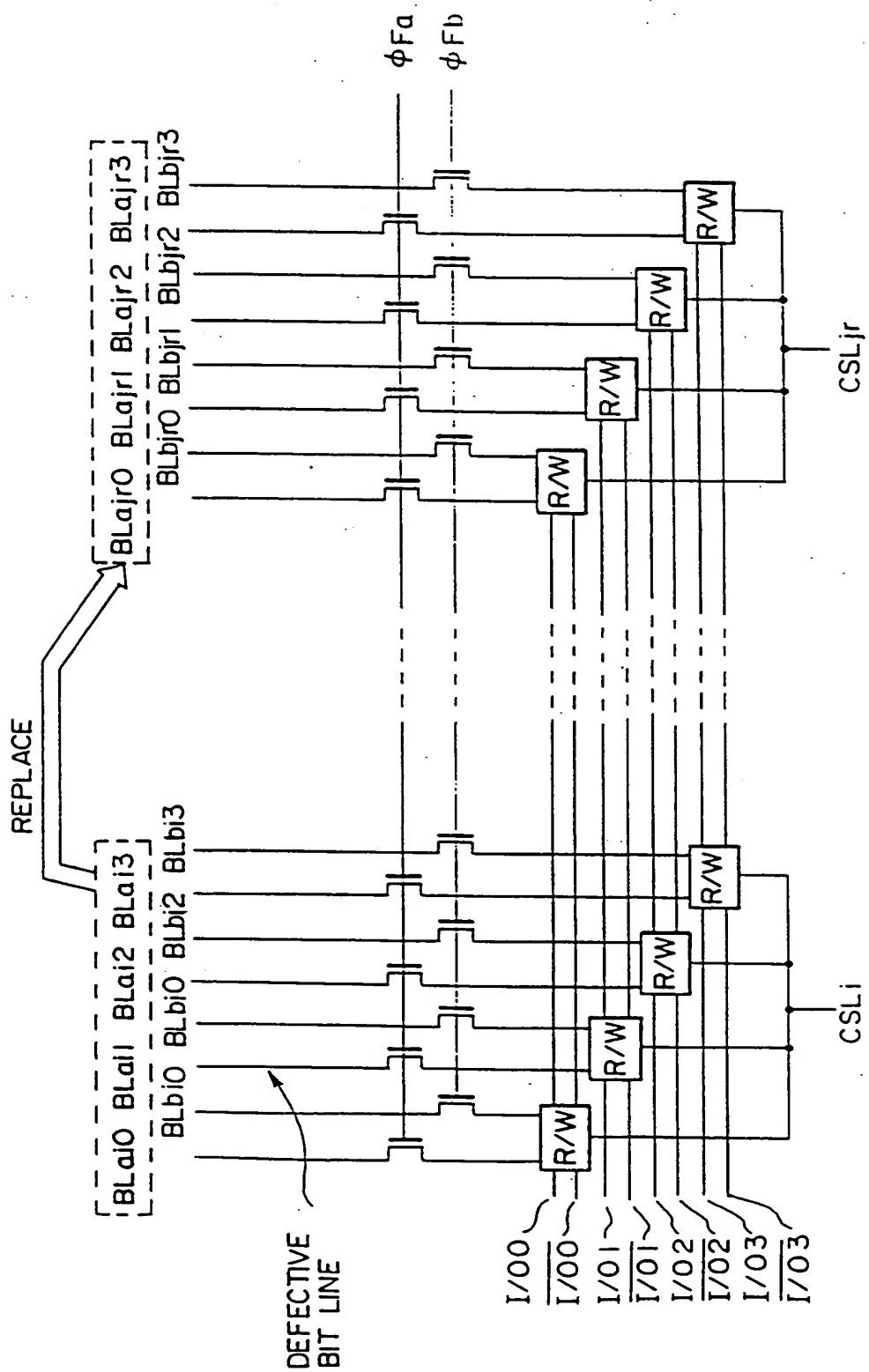


FIG. 43

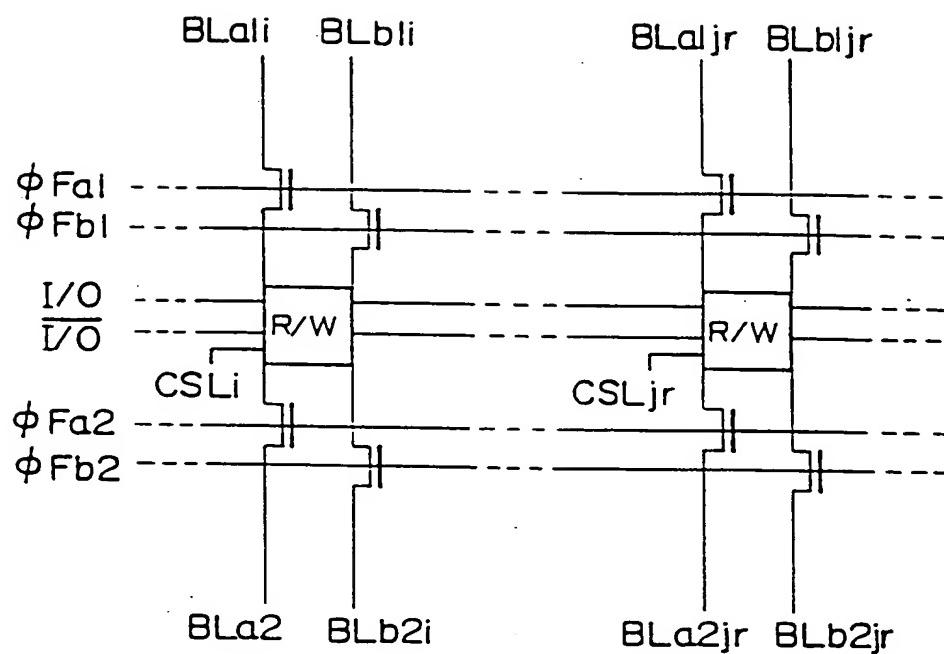


FIG. 44

FIG. 45(a)

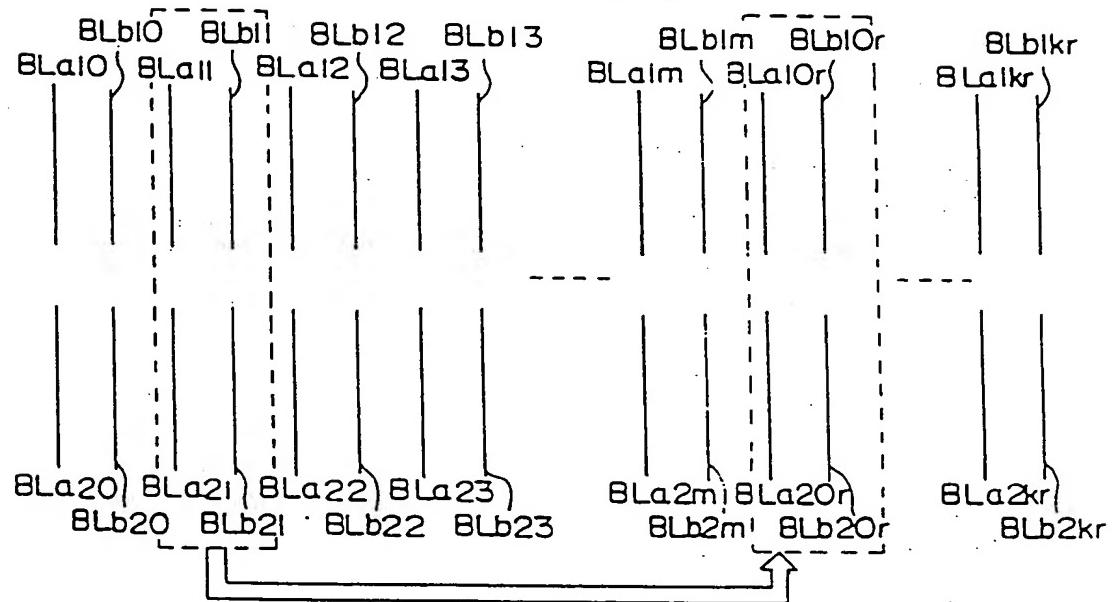


FIG. 45(b)

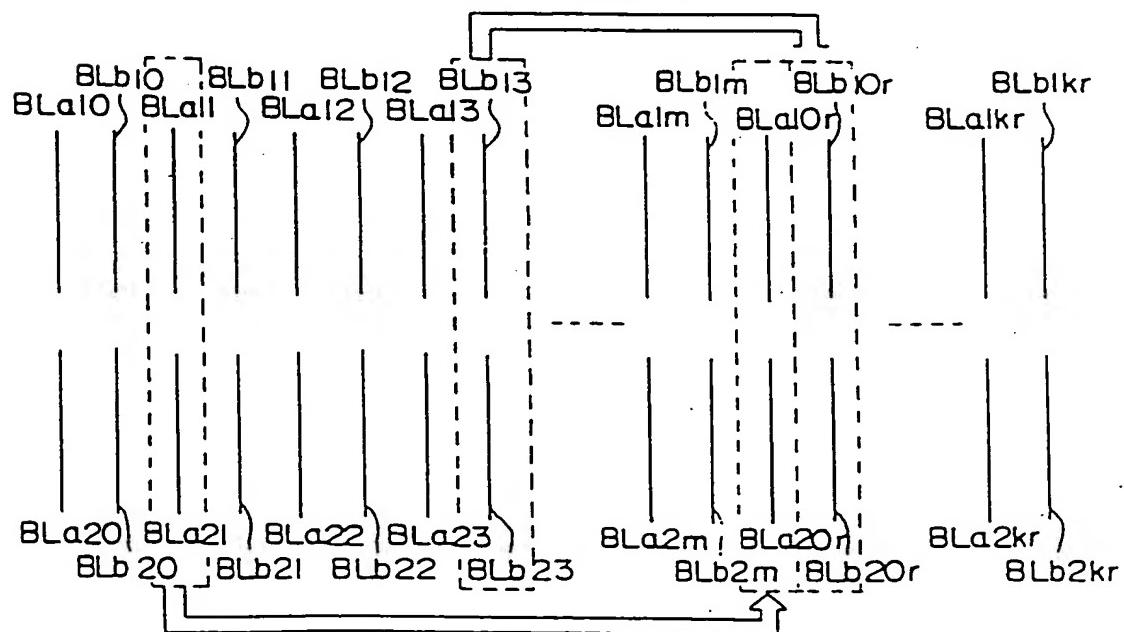


FIG. 46(a)

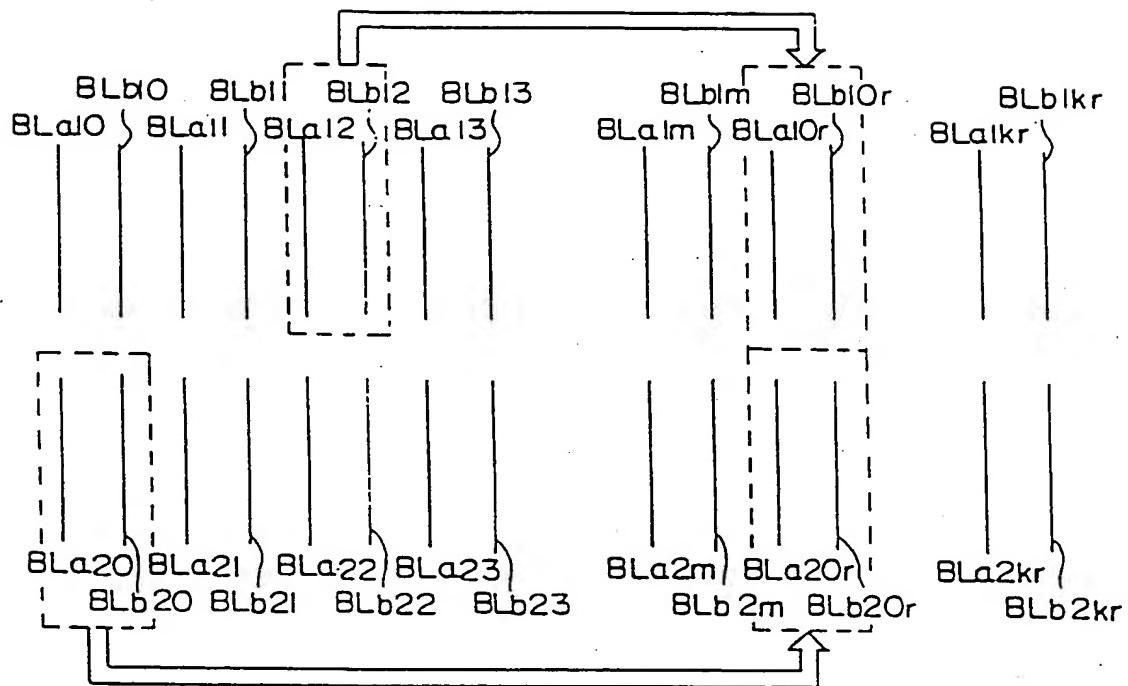
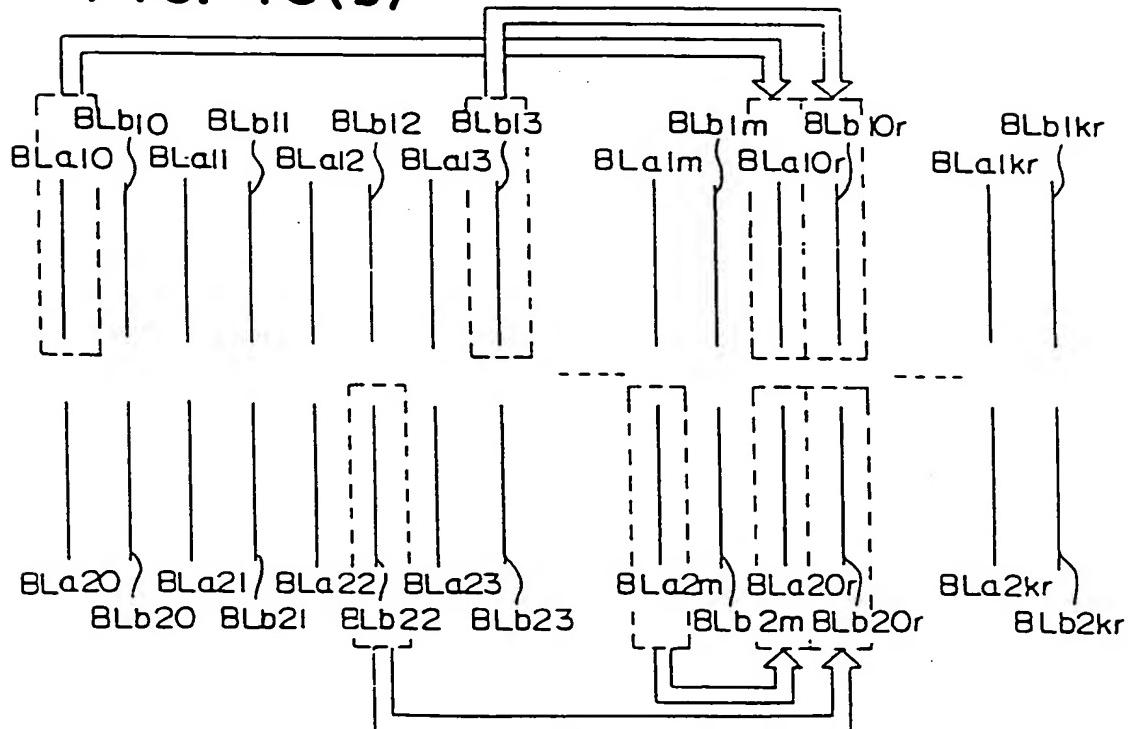


FIG. 46(b)



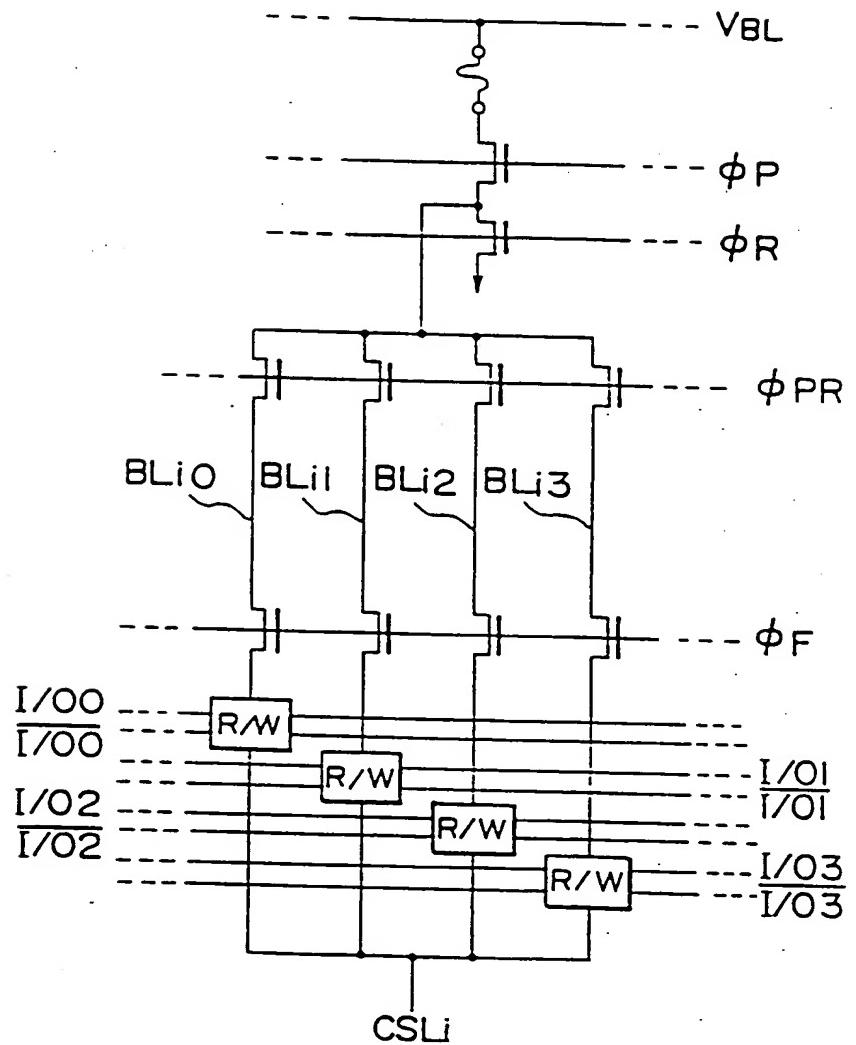


FIG. 47

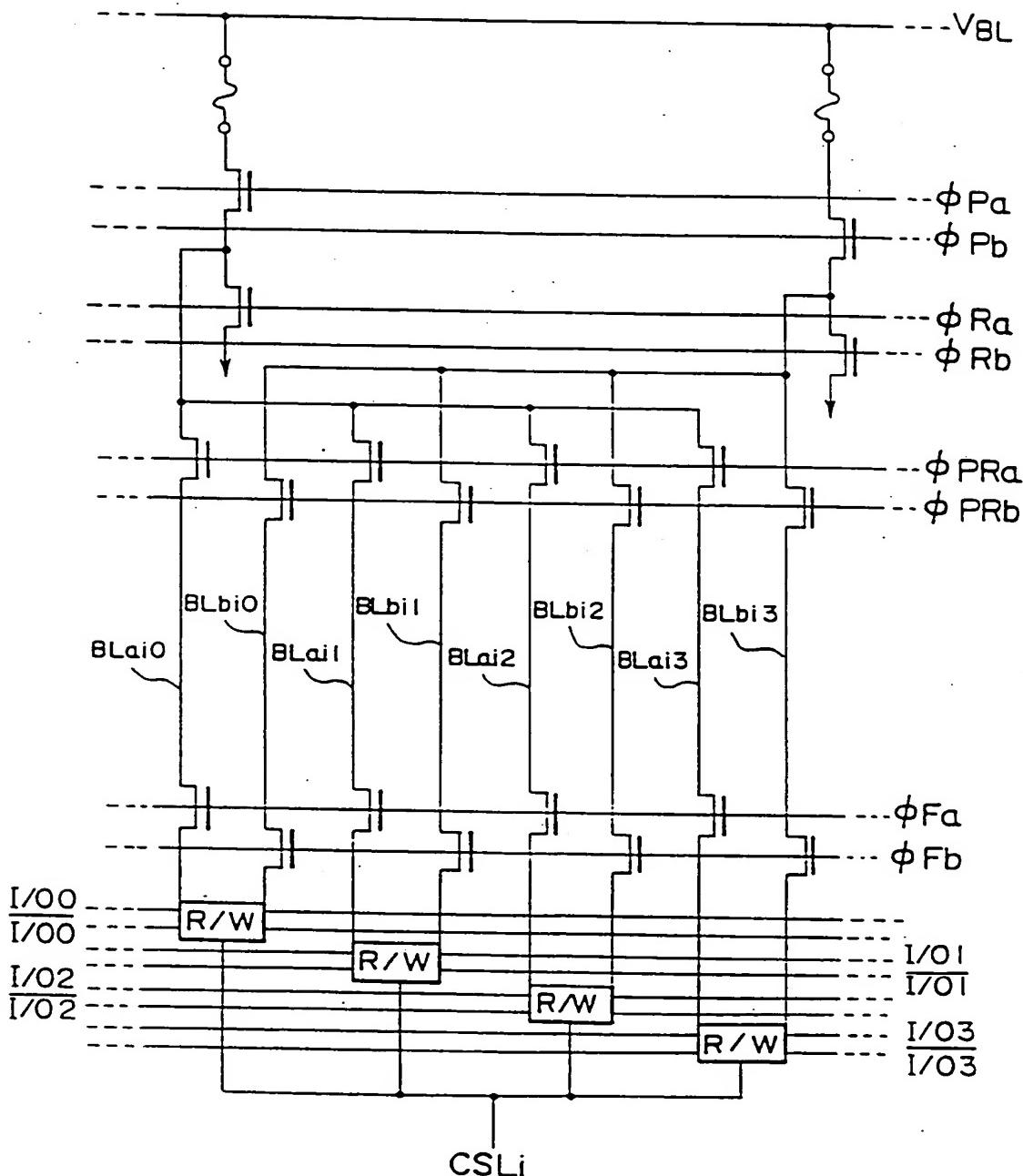


FIG. 48

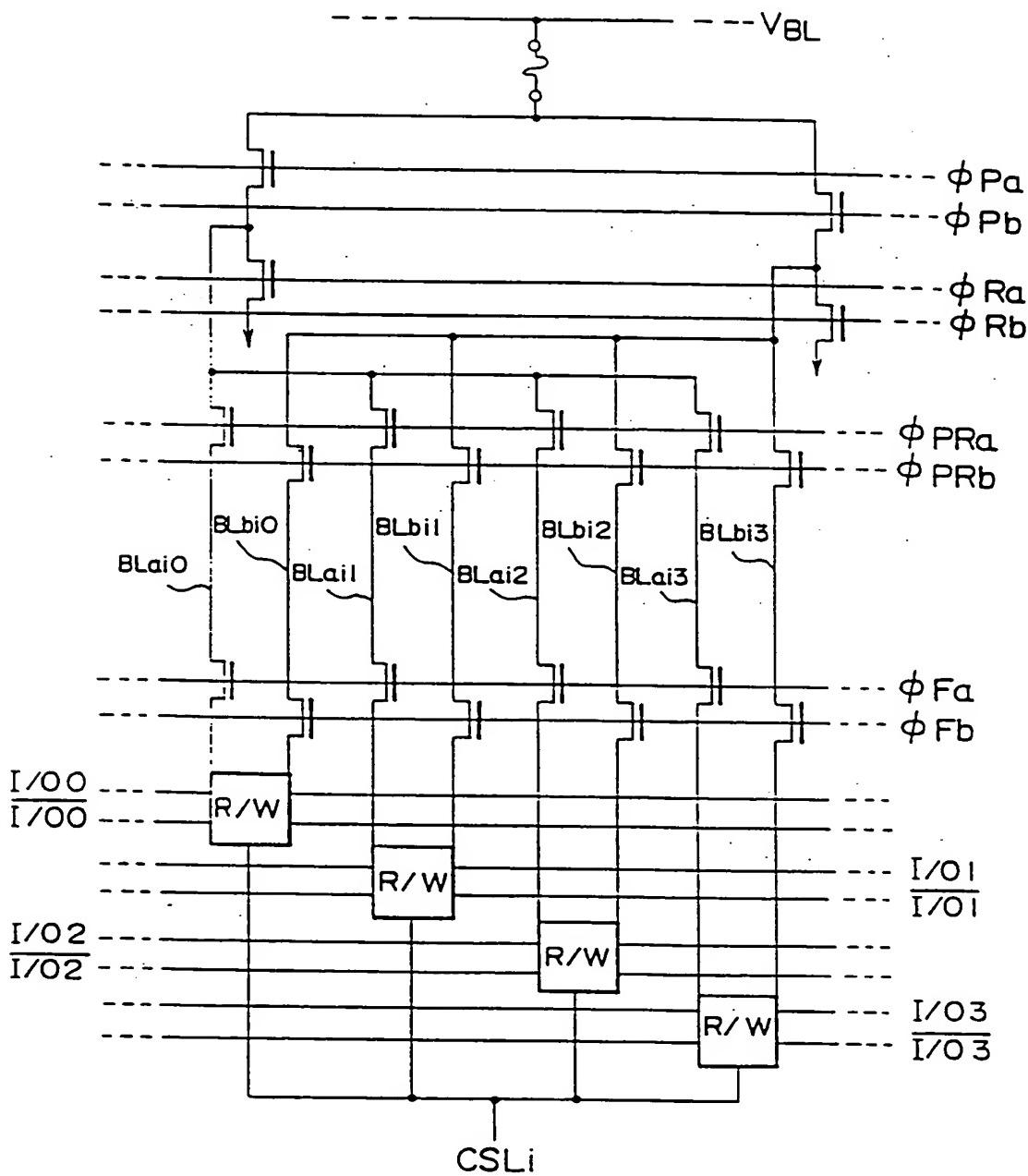


FIG. 49

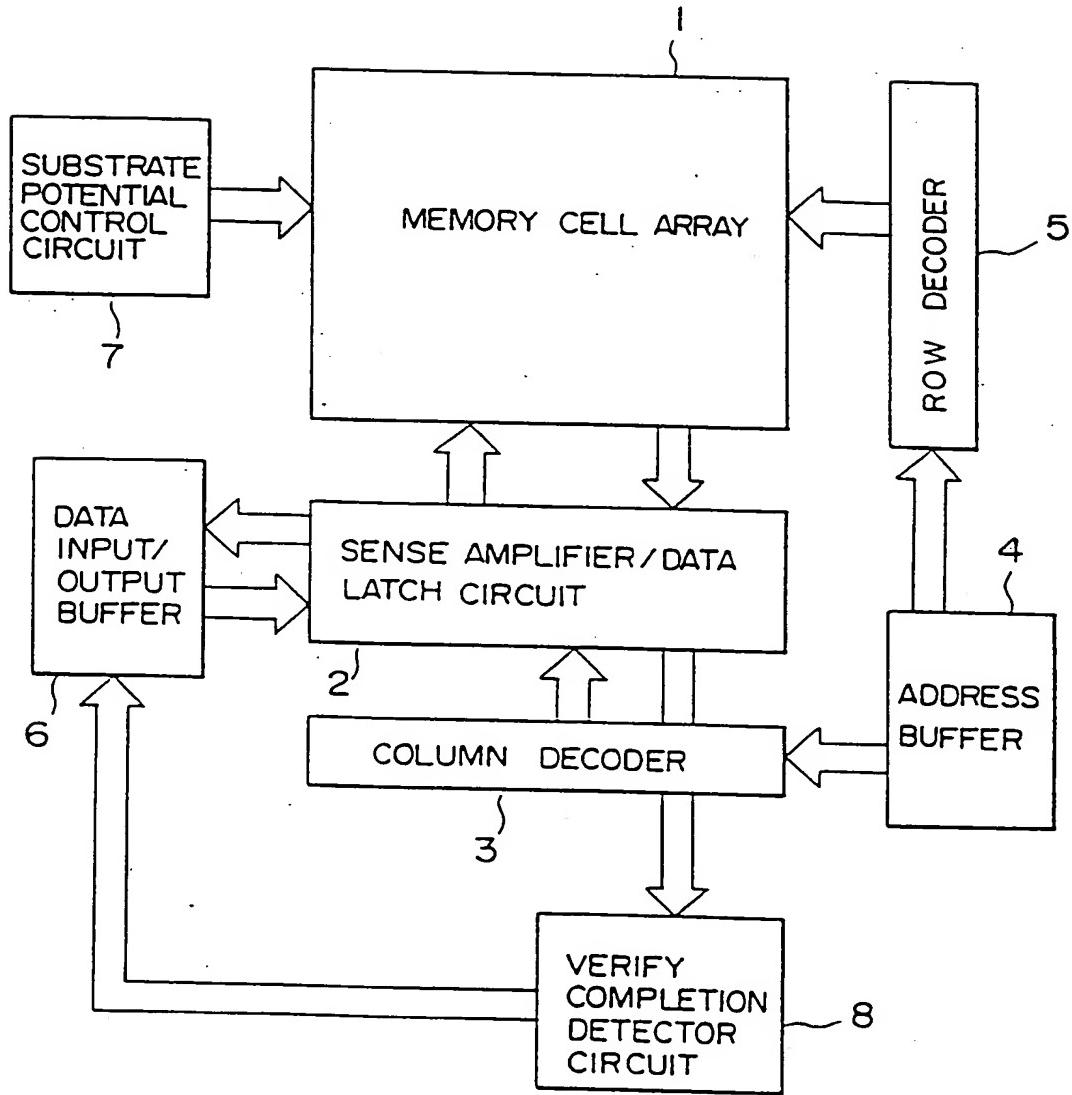


FIG. 50

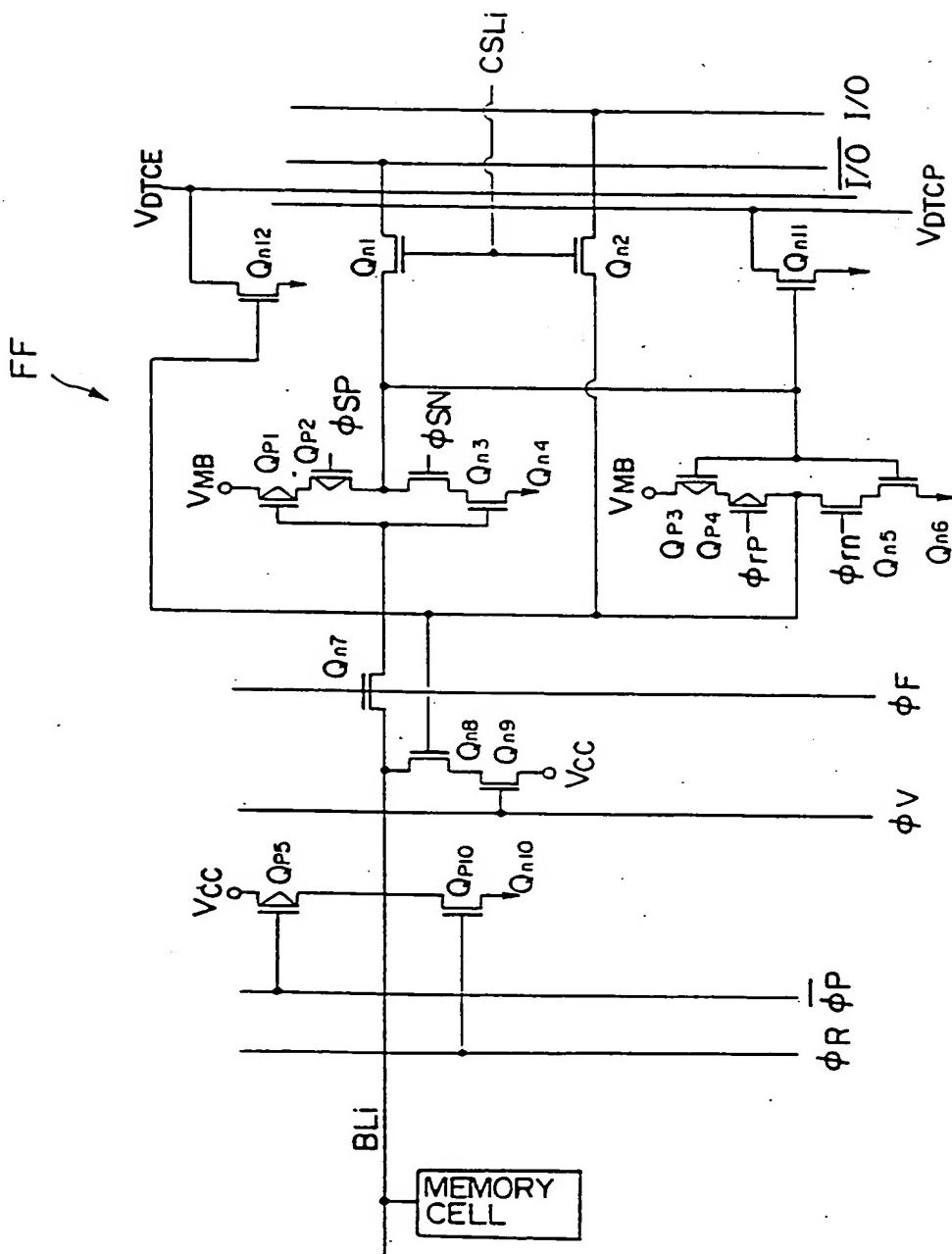


FIG. 51

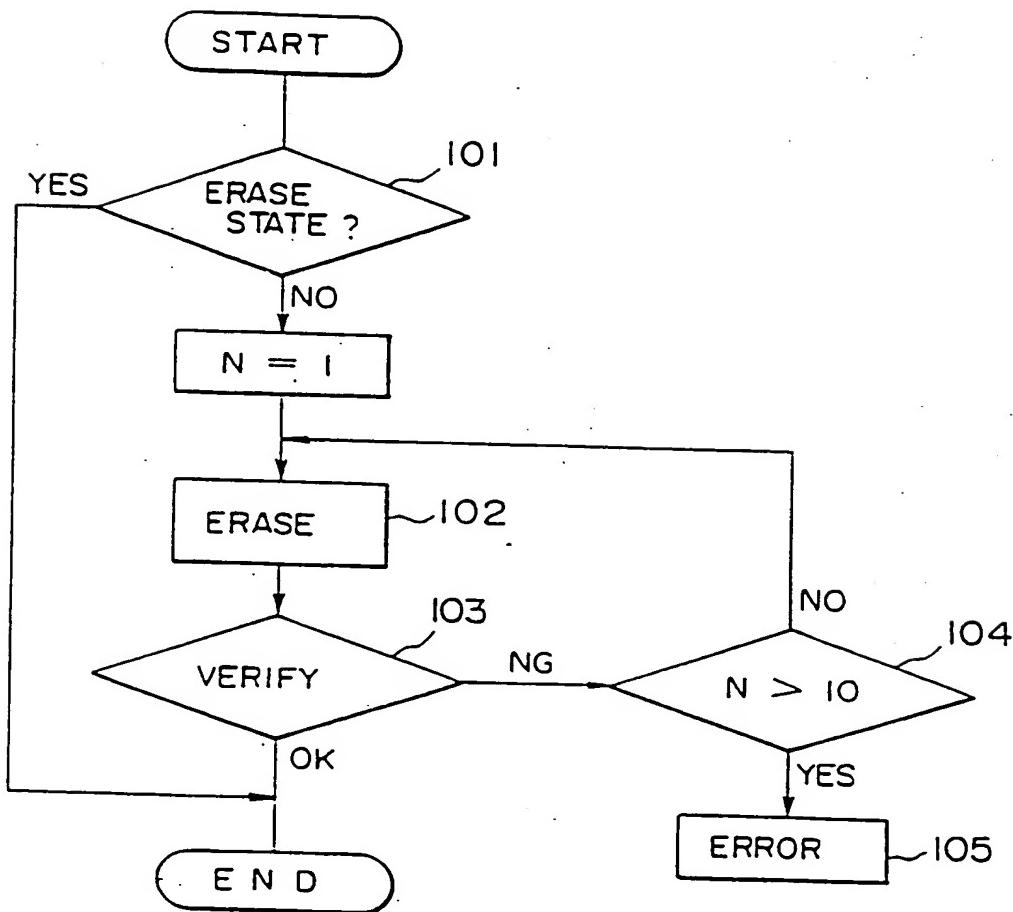


FIG. 52

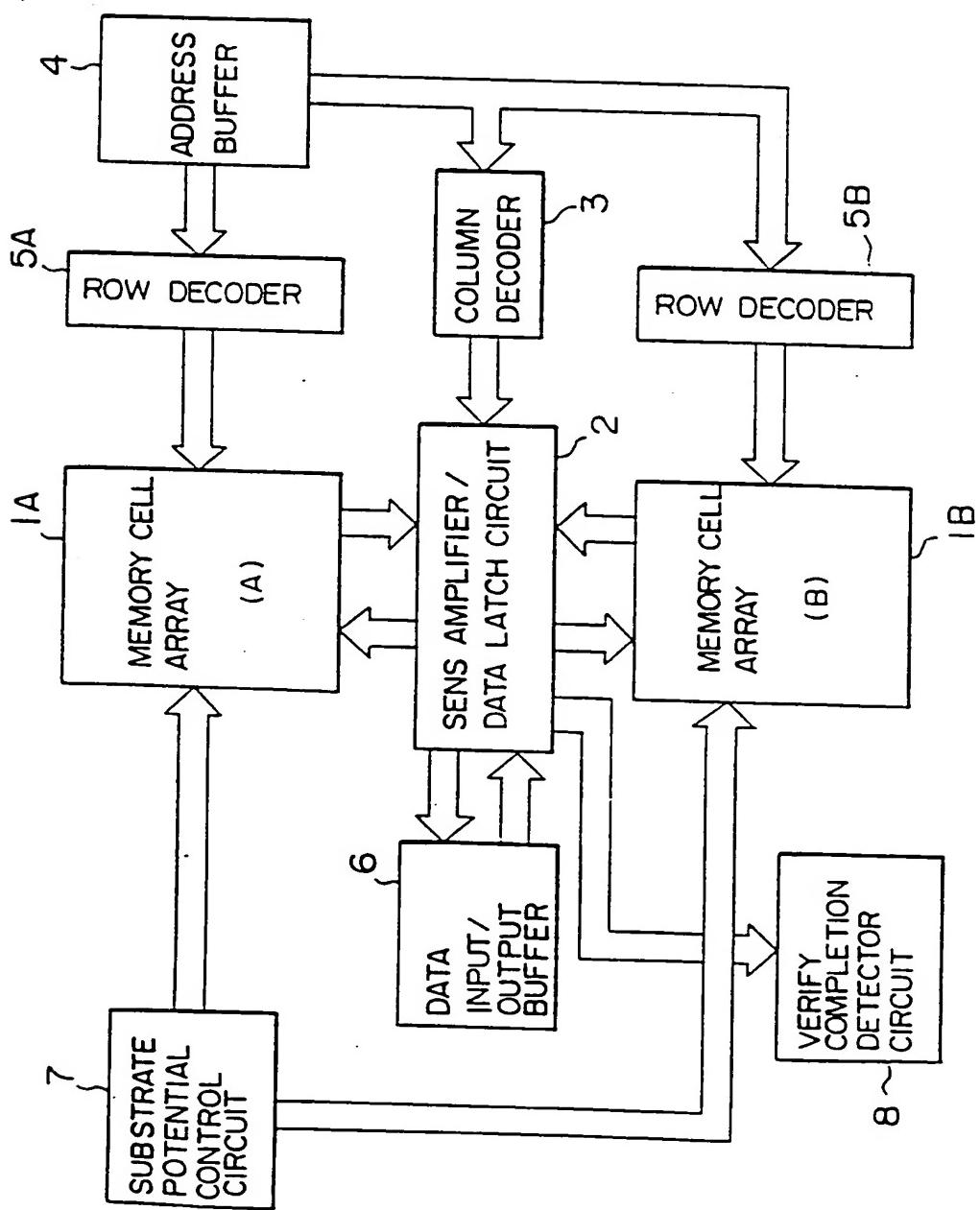


FIG. 53

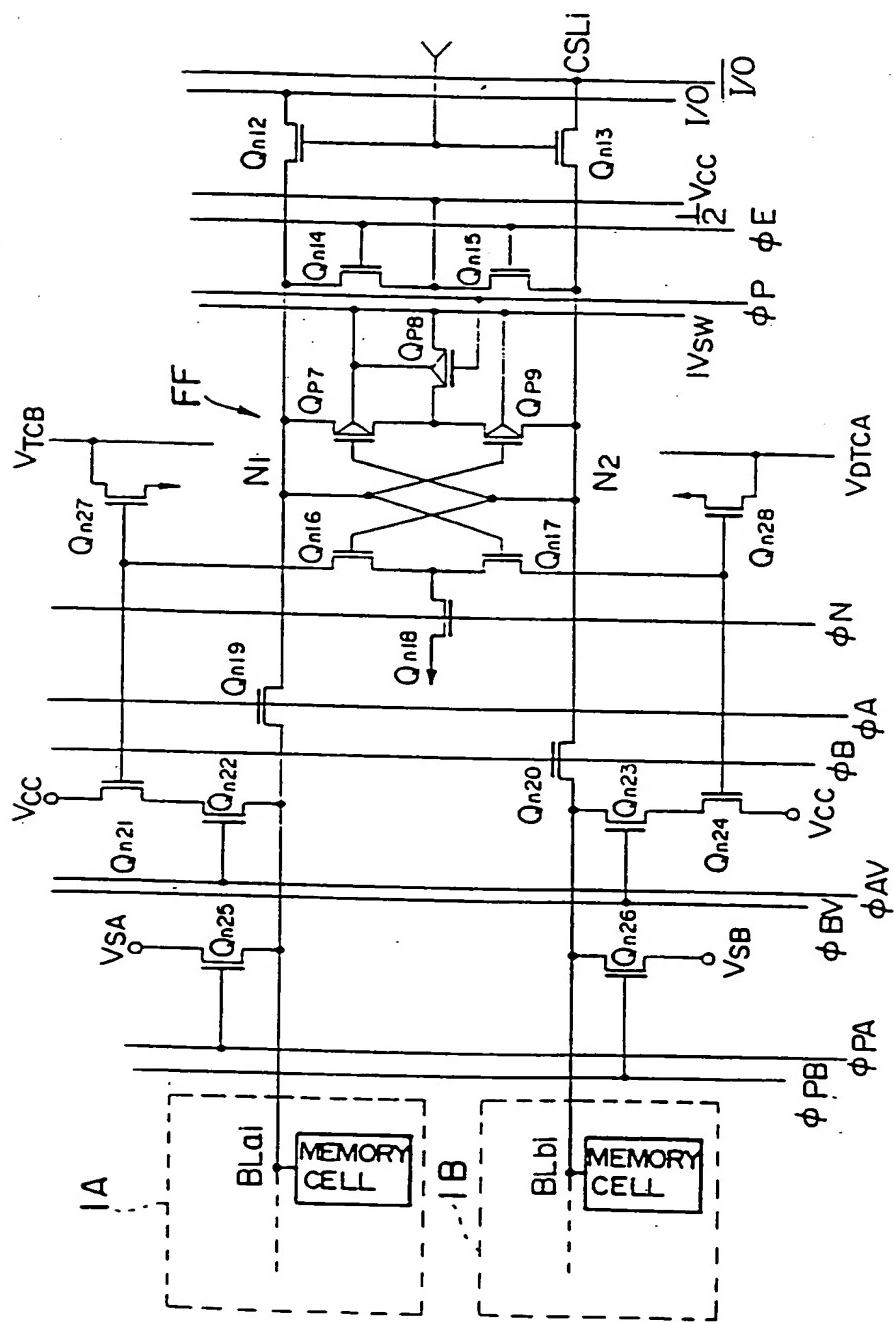


FIG. 54

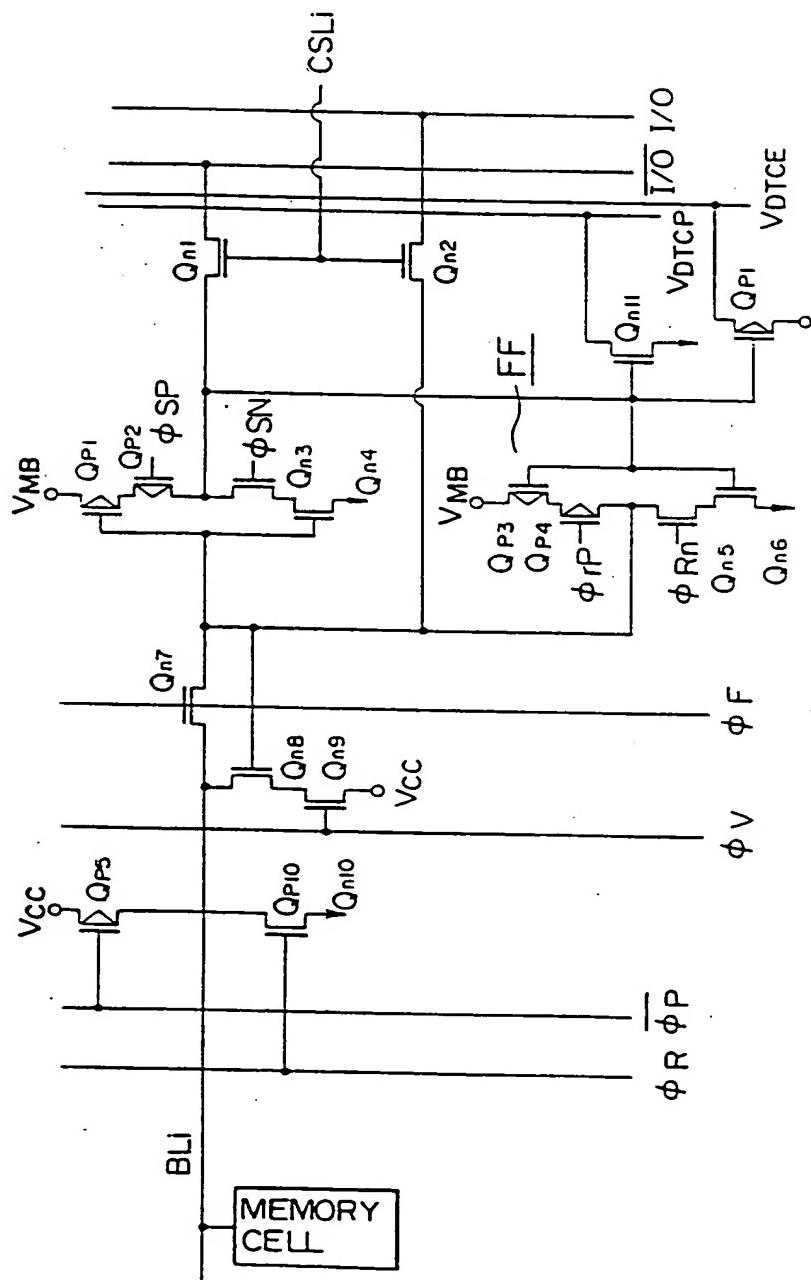


FIG. 55

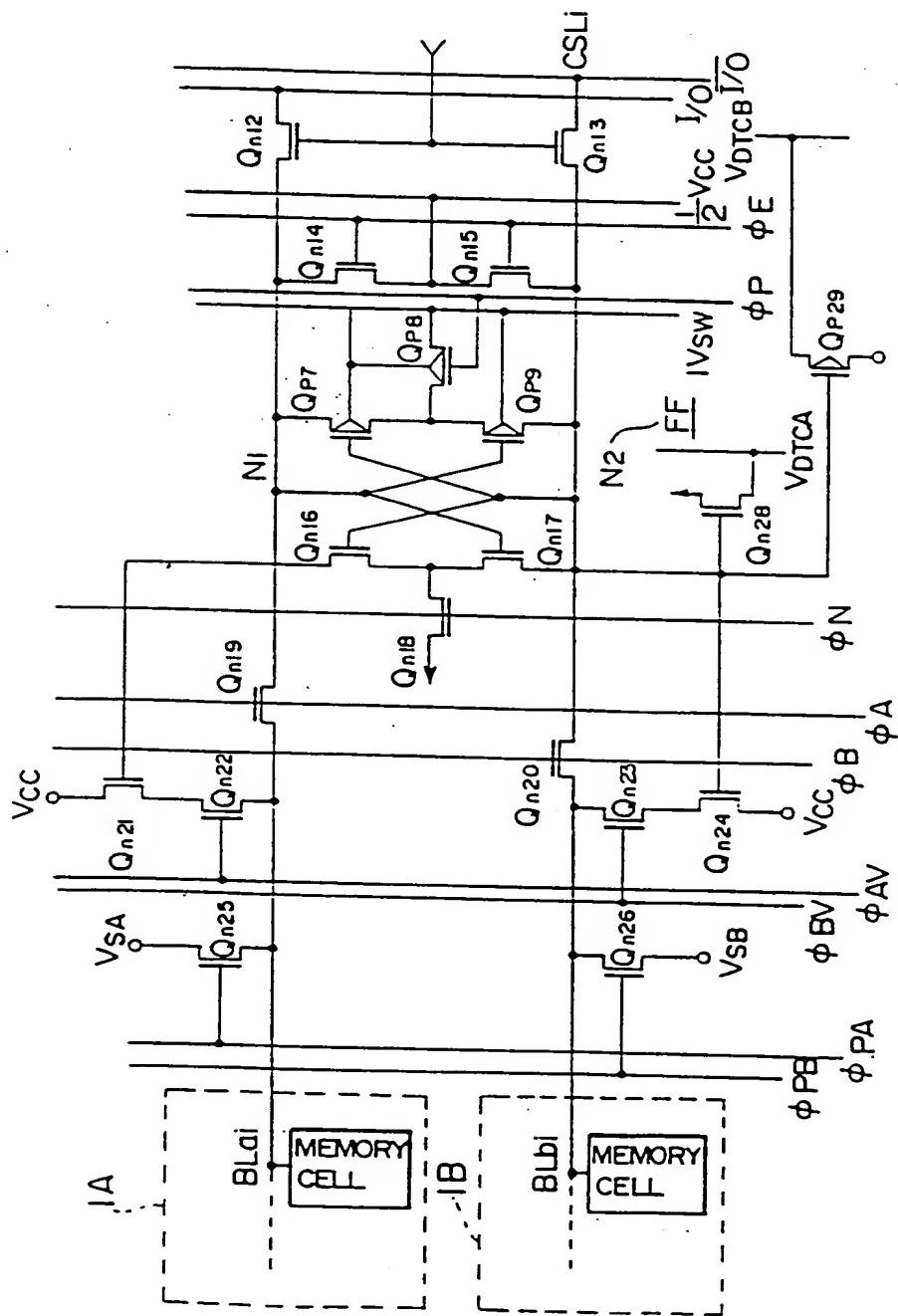


FIG. 56

FIG. 57(a)

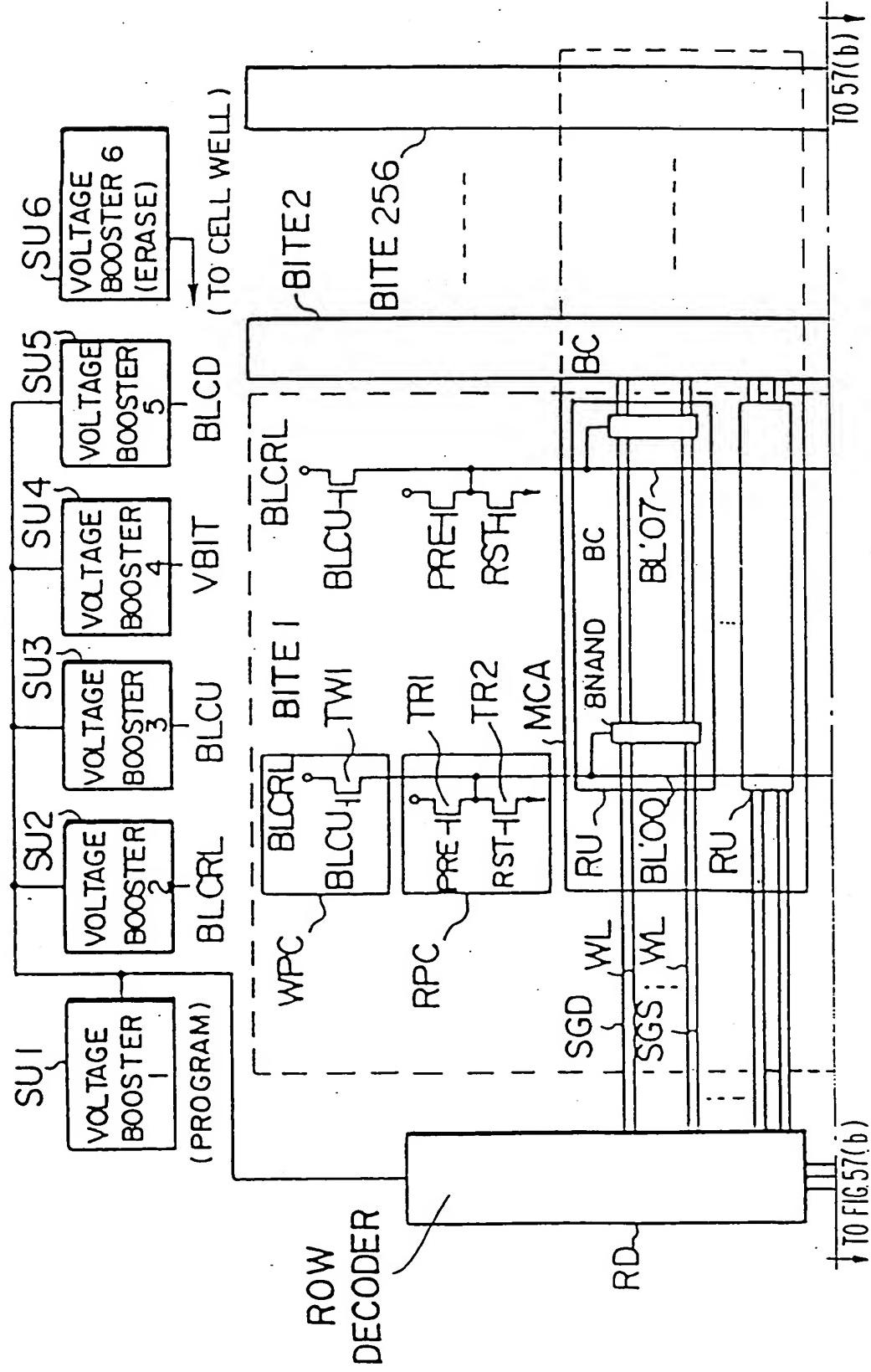


FIG. 57(b)

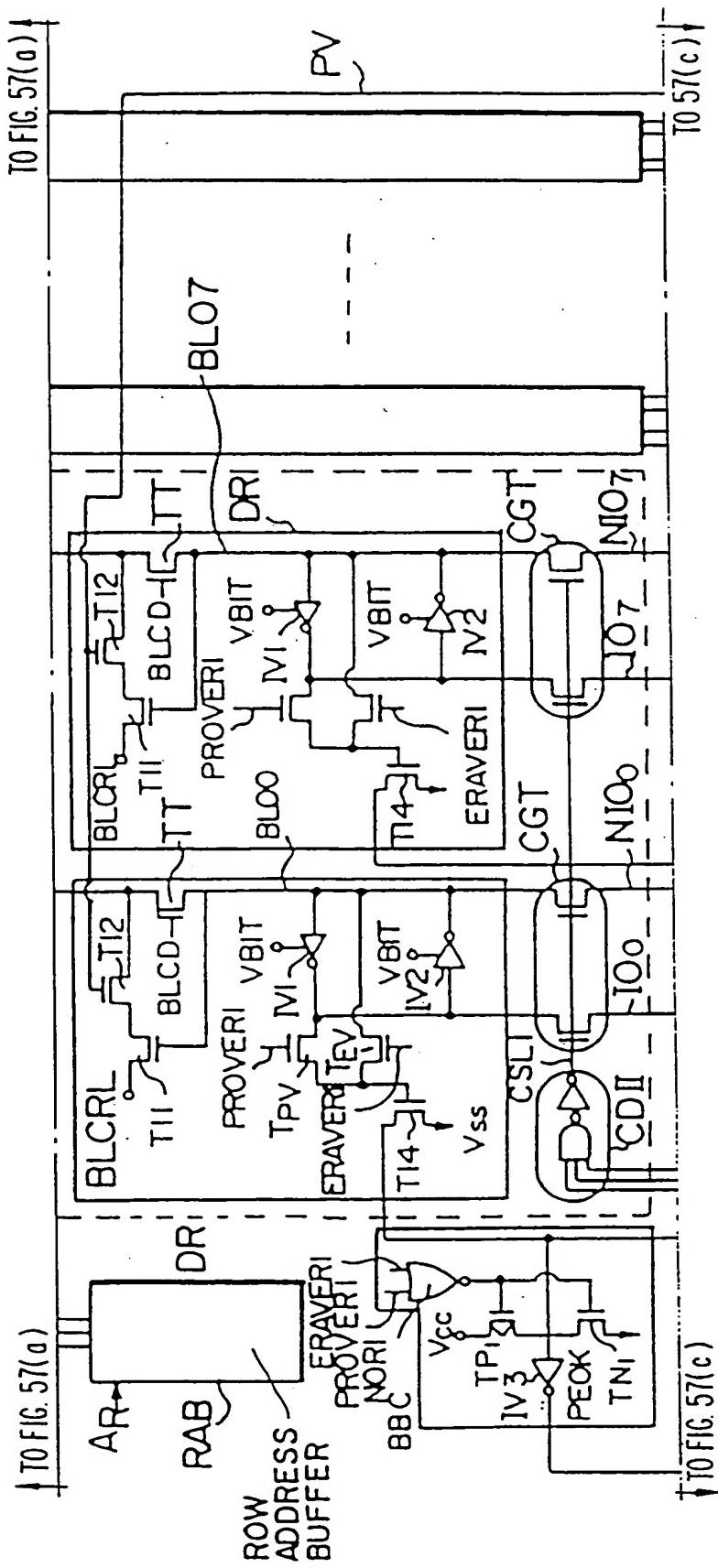
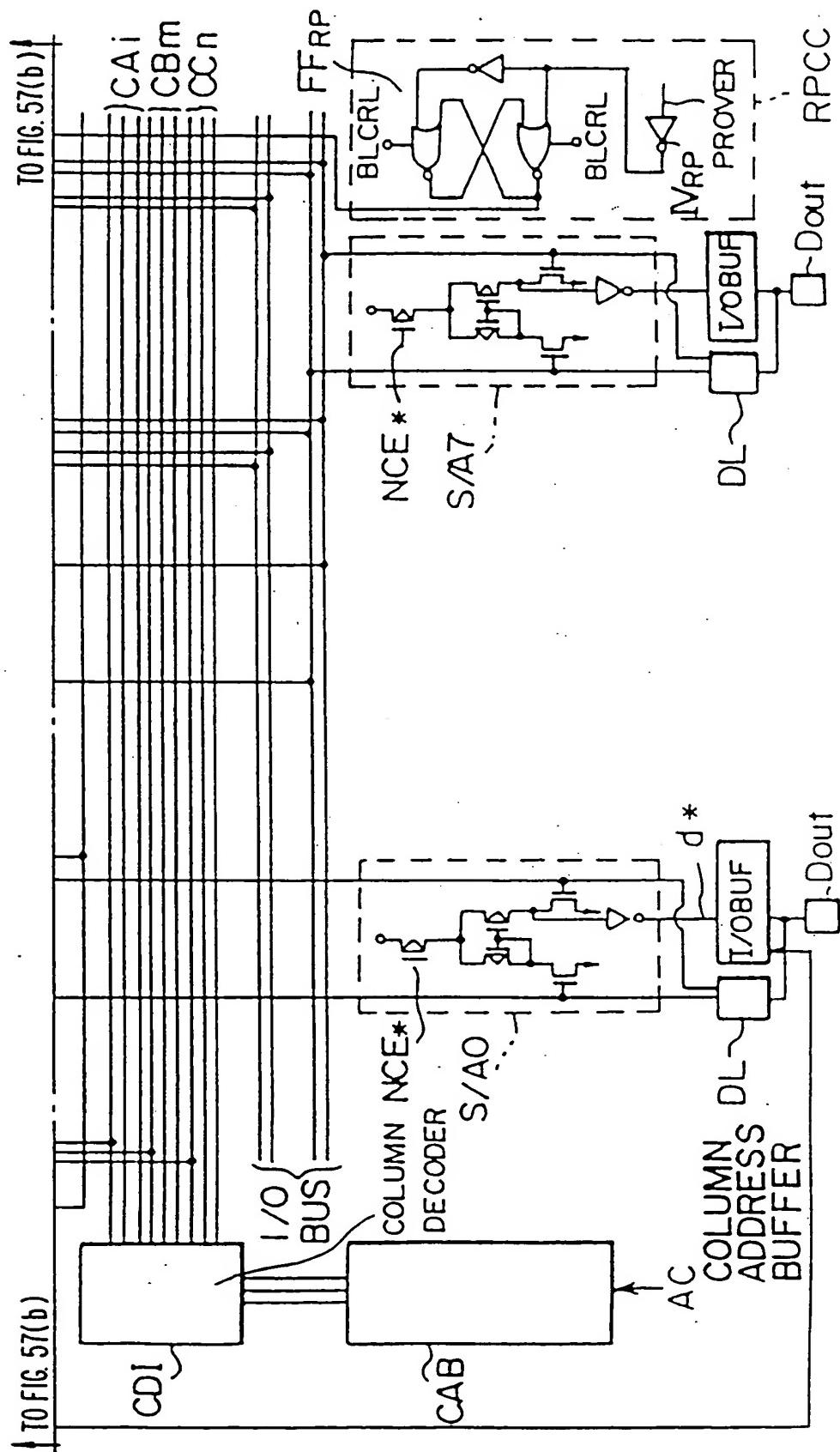


FIG. 57(c)



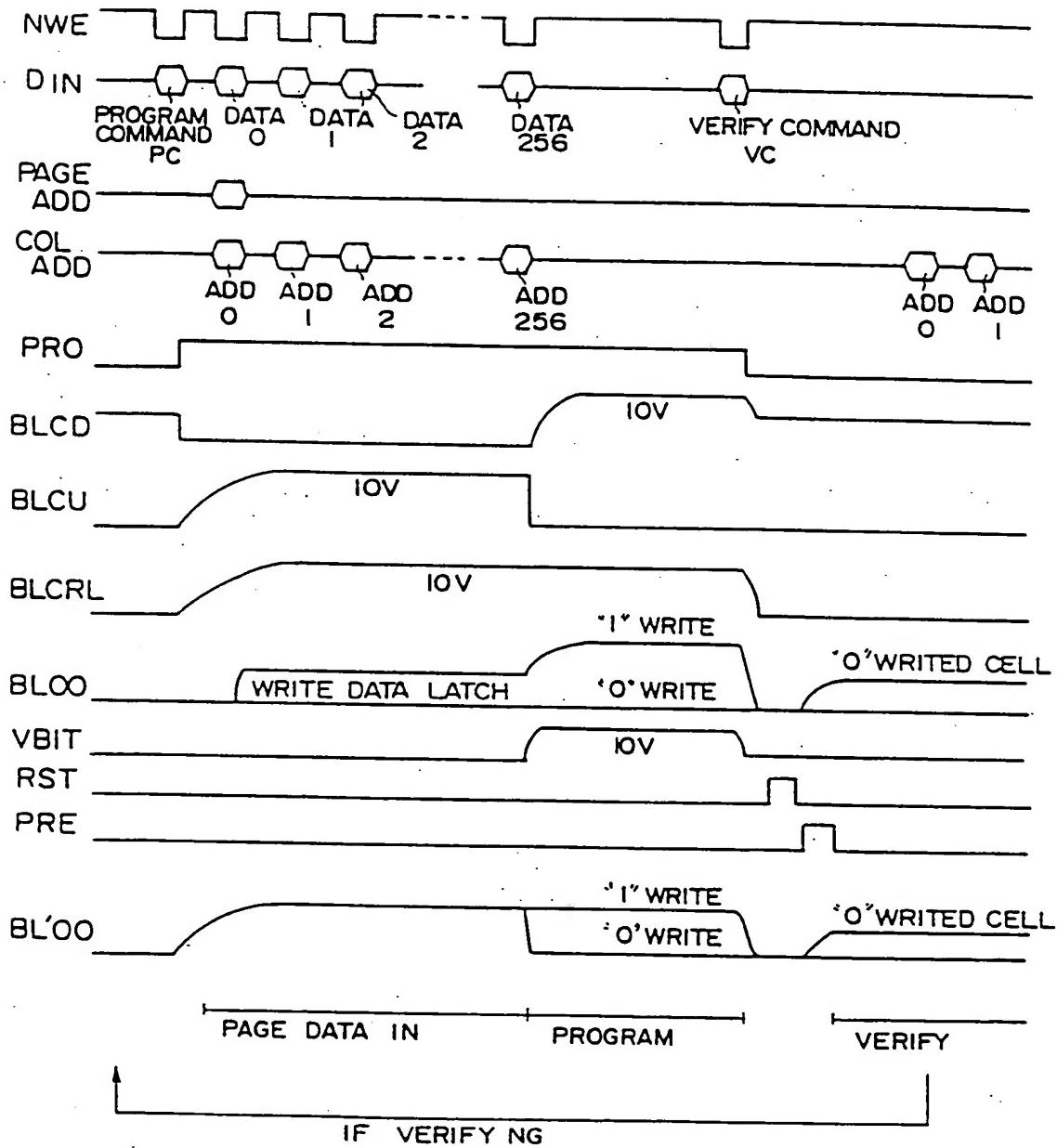


FIG. 58

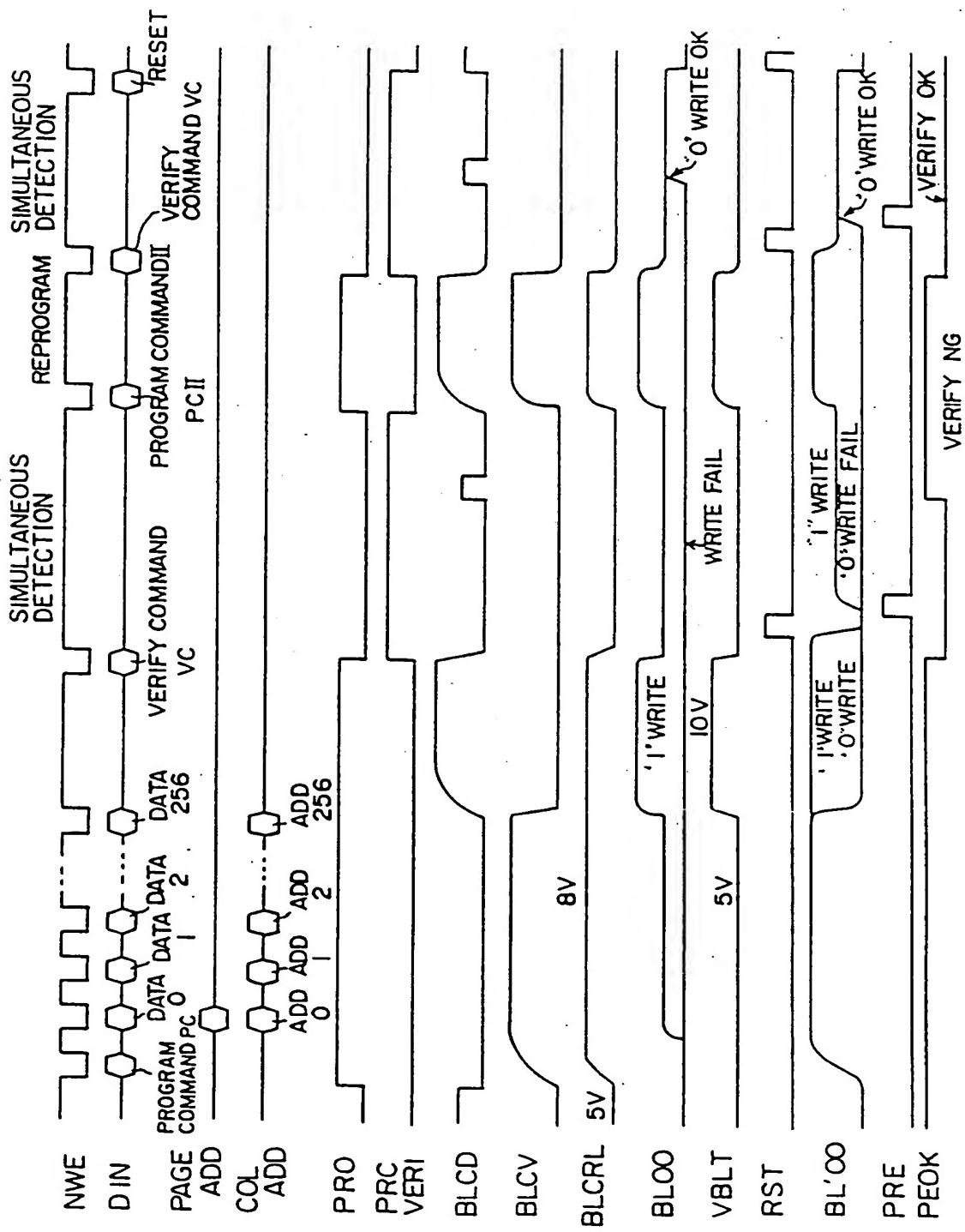


FIG. 59

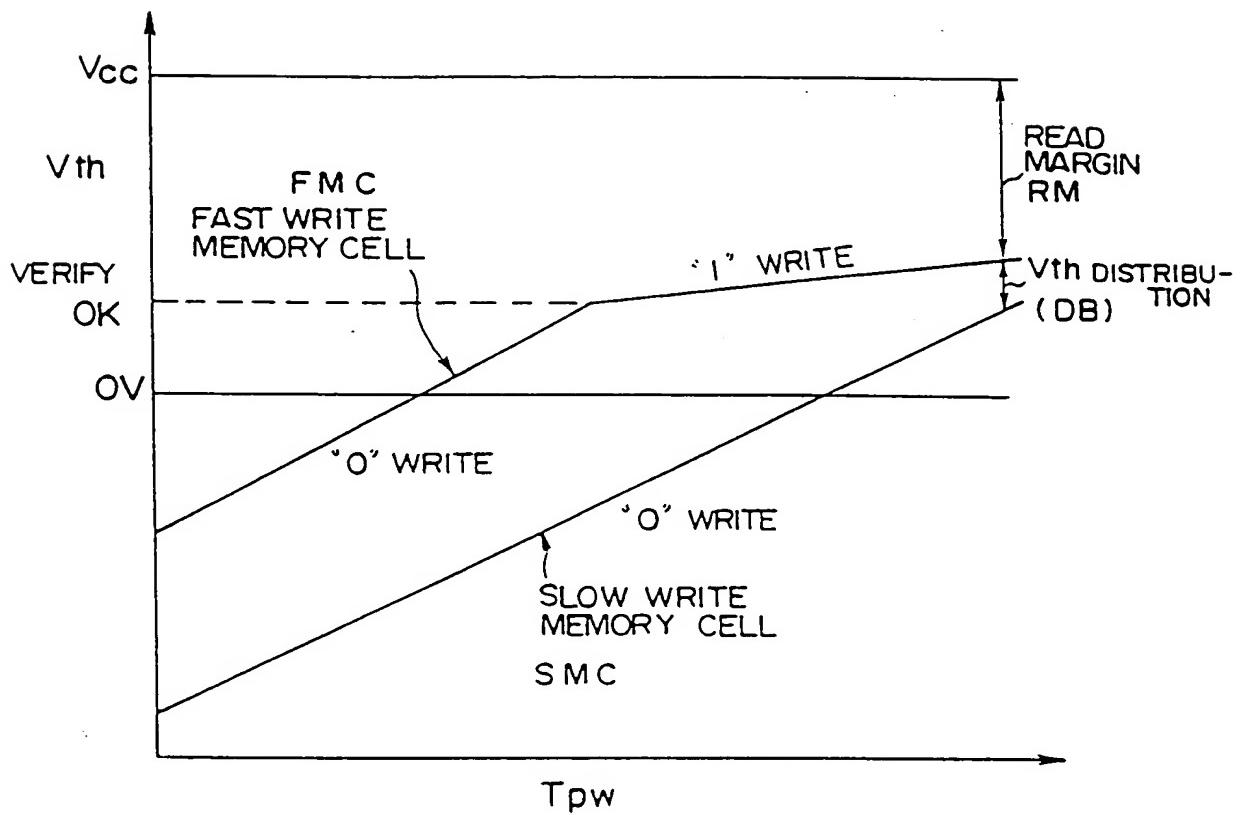


FIG. 60

(ERASE FLOW CHART)

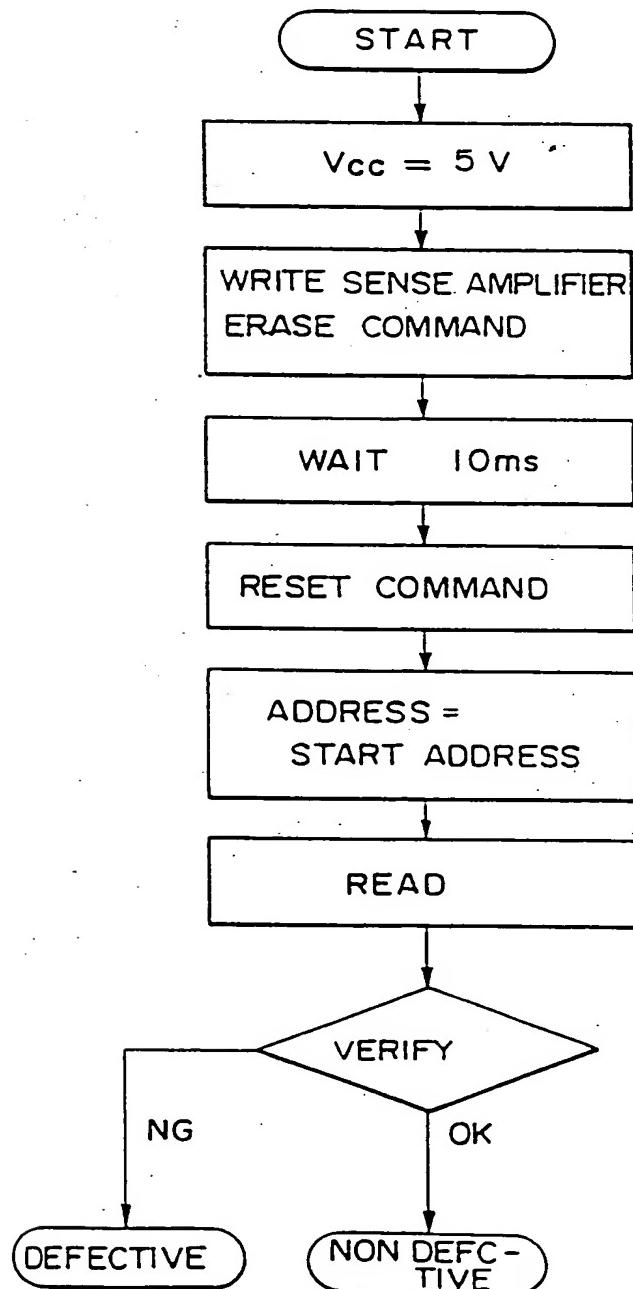


FIG. 61

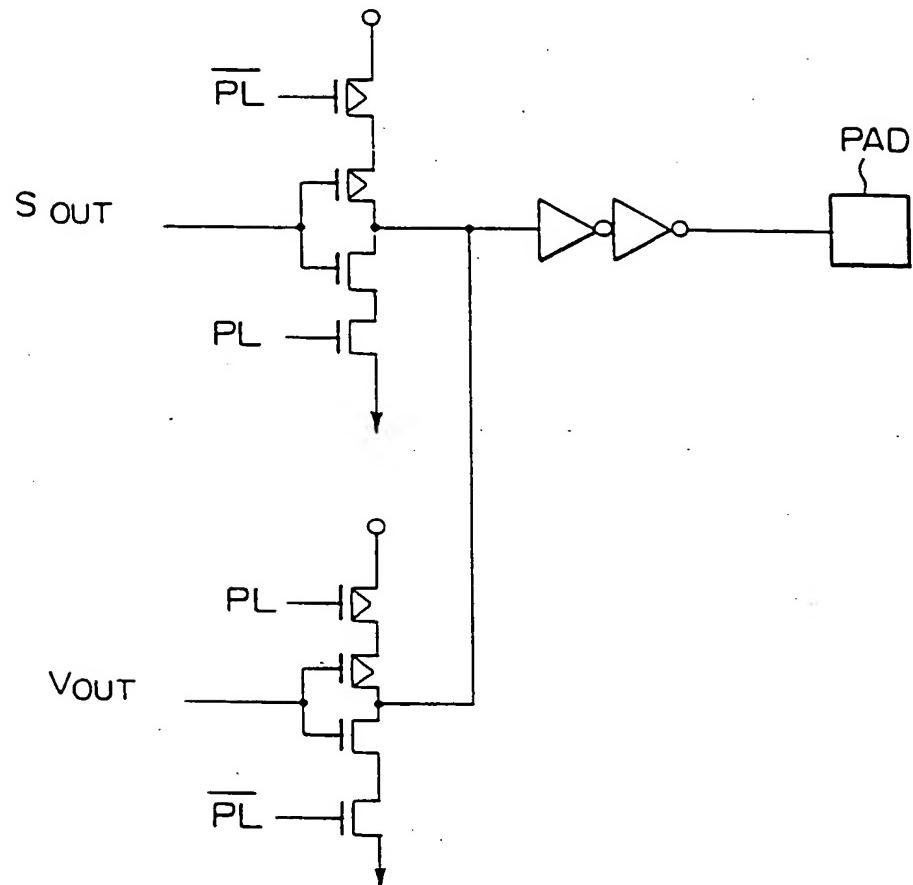


FIG. 62

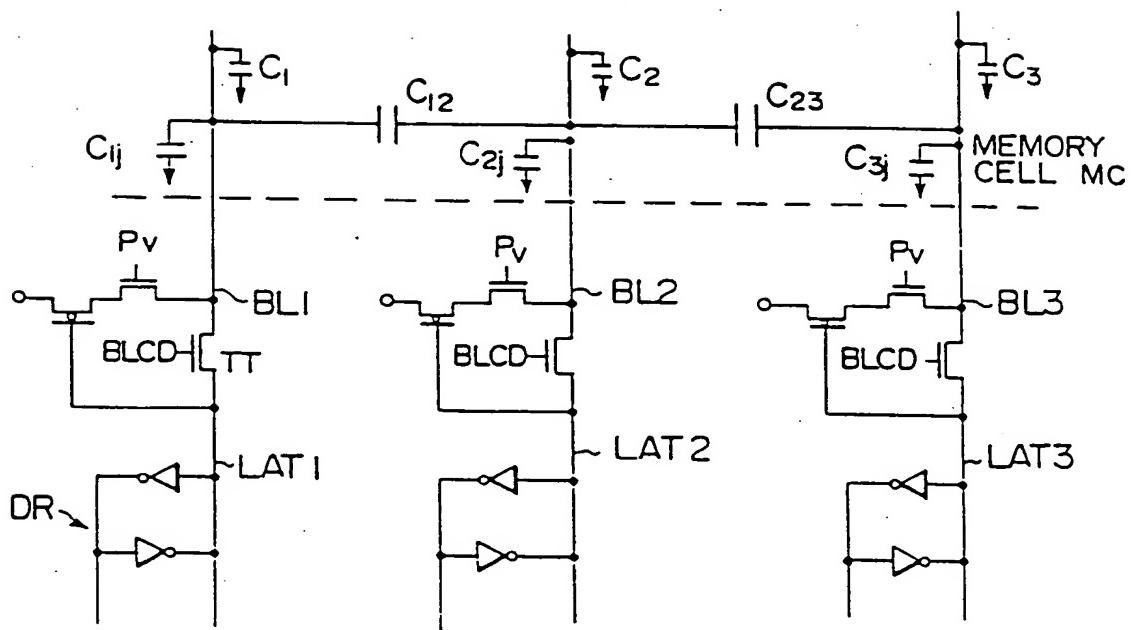


FIG. 63

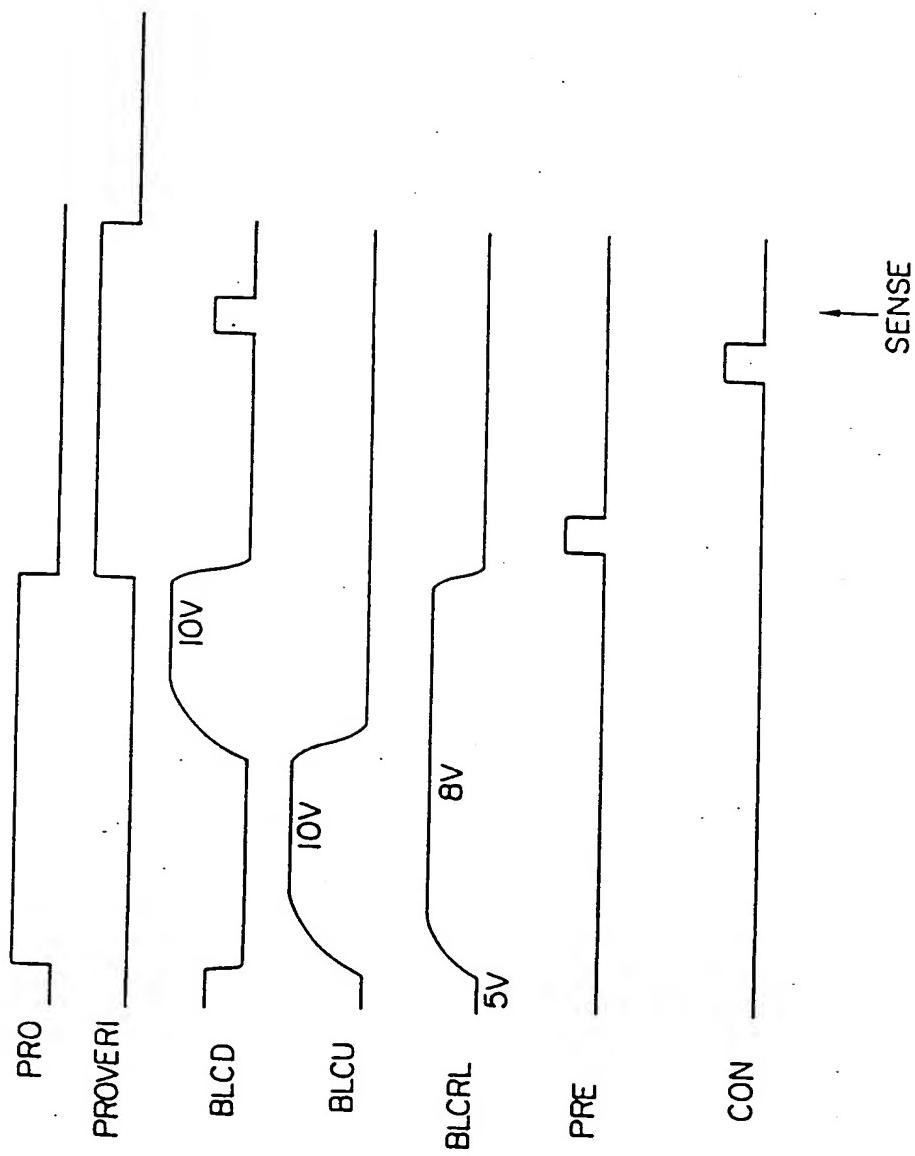


FIG. 64

FIG. 65(a)

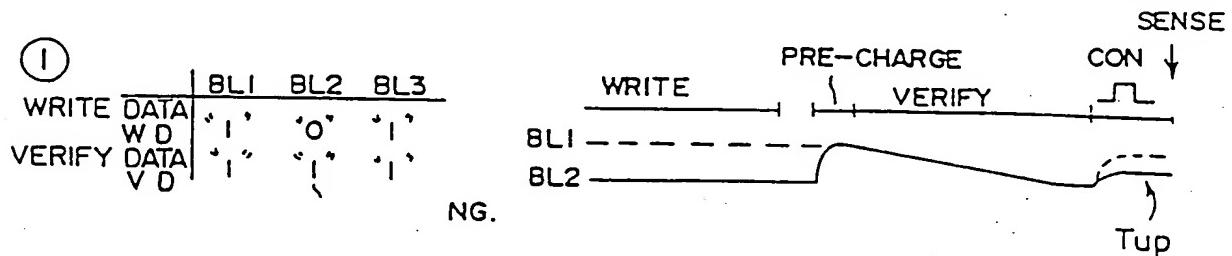


FIG. 65(b)

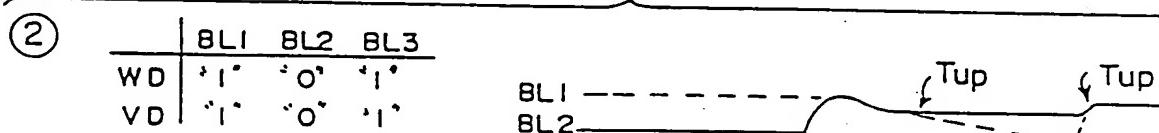


FIG. 65(c)

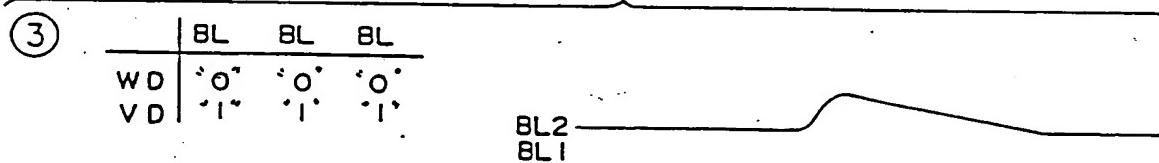


FIG. 65(d)

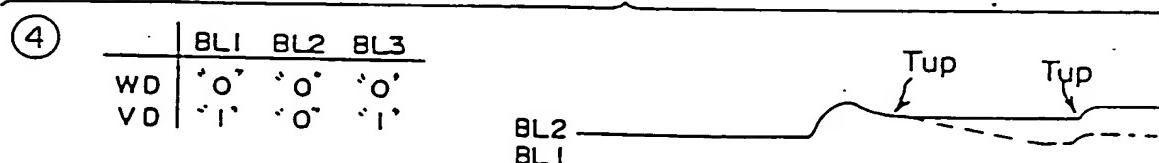


FIG. 65(e)

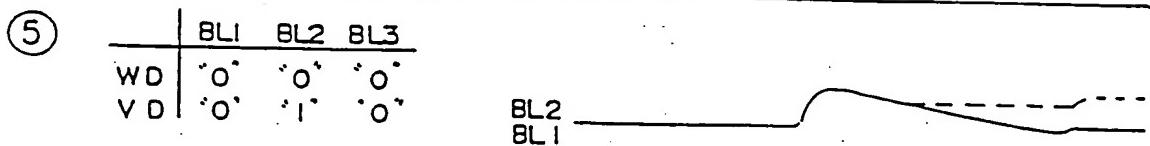


FIG. 65(f)

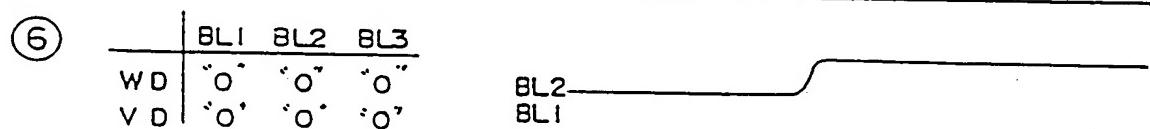


FIG. 65(g)

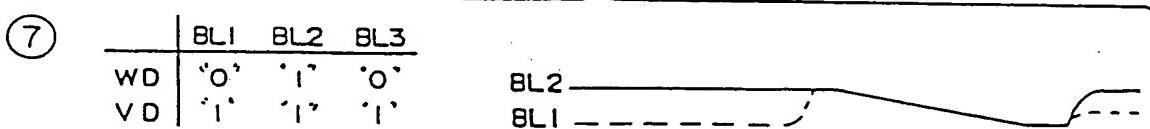


FIG. 65(h)

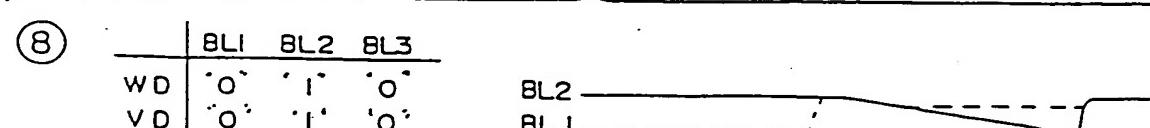


FIG. 66(a)

	BL1	BL2	BL3
WD	'1'	'0'	'1'
VD	'1'	'1'	'1'

FIG. 66(b)

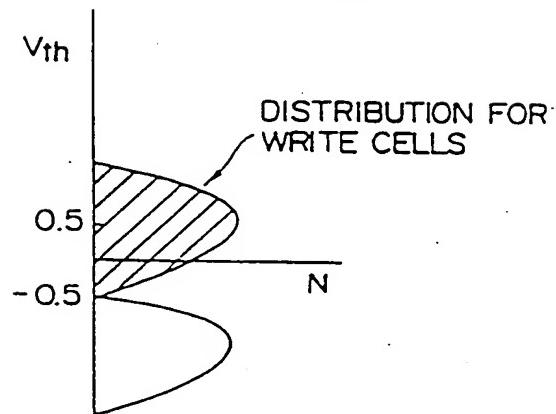
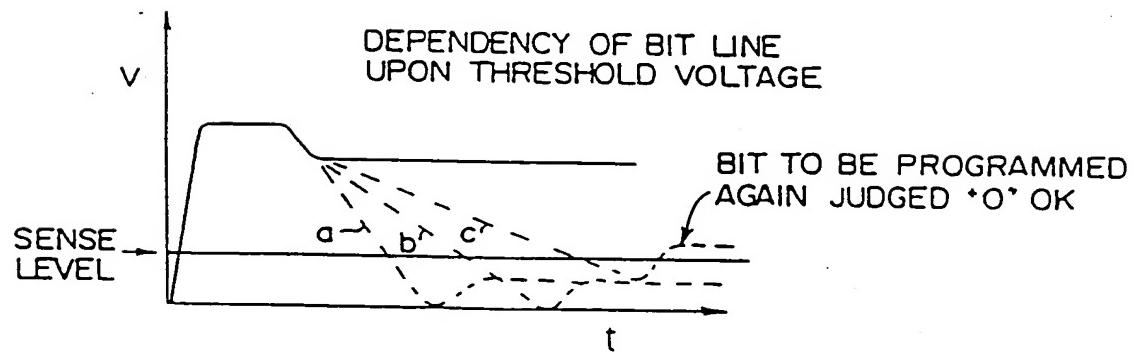


FIG. 66(c)



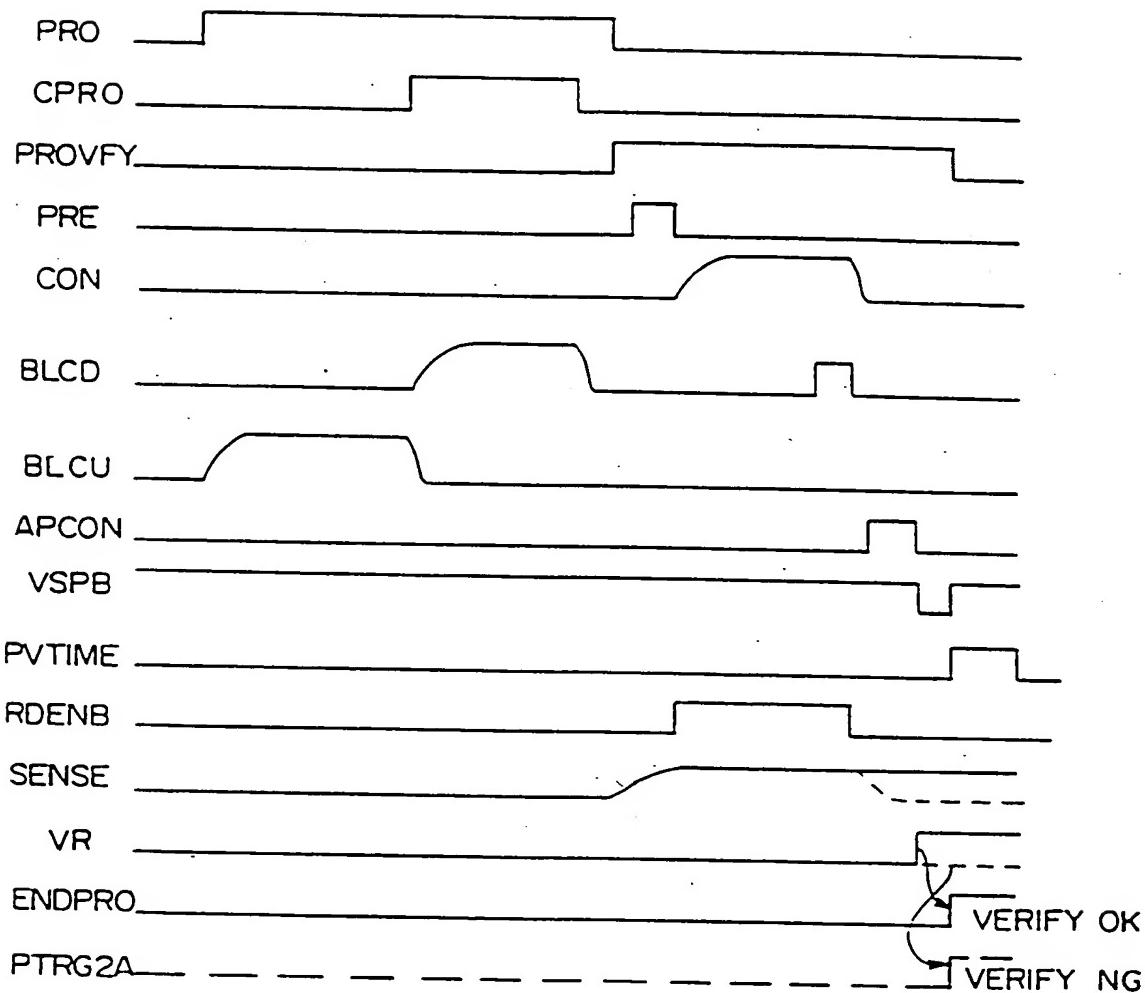


FIG. 67

FIG. 68(a)

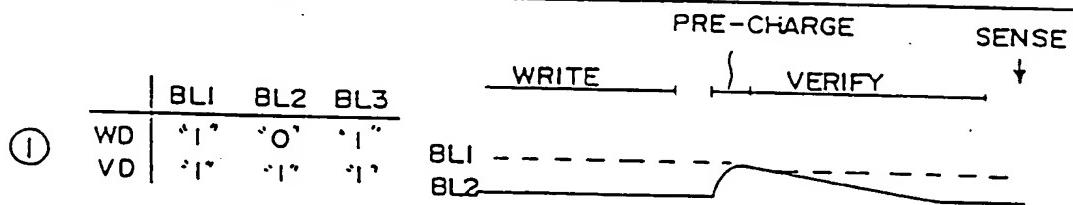


FIG. 68(b)

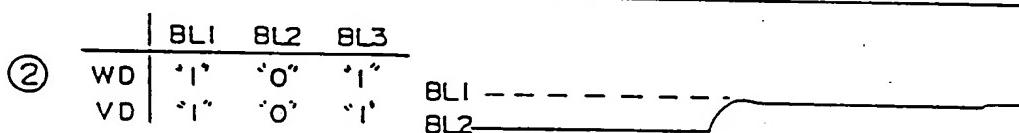


FIG. 68(c)

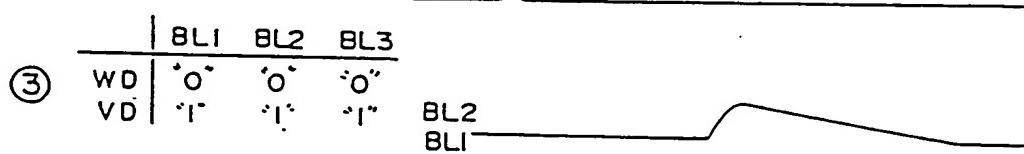


FIG. 68(d)

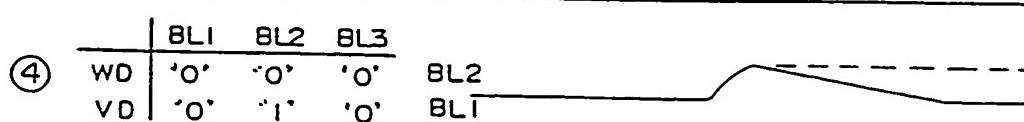


FIG. 68(e)

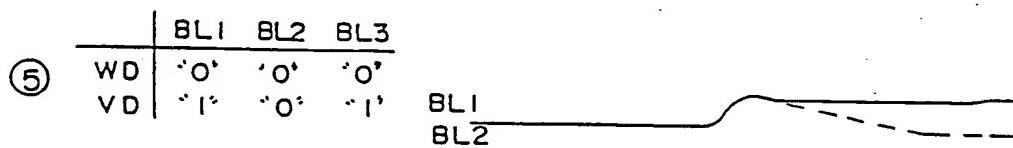


FIG. 68(f)

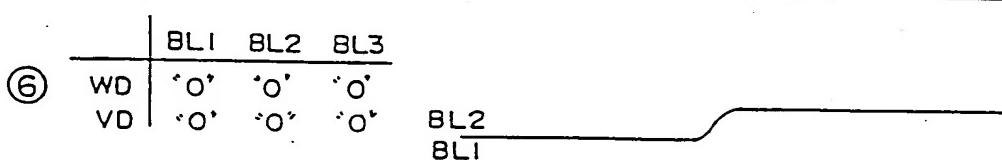


FIG. 68(g)

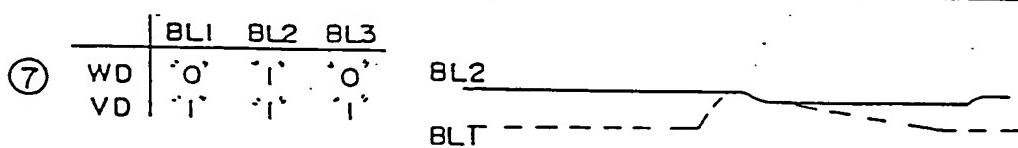


FIG. 68(h)

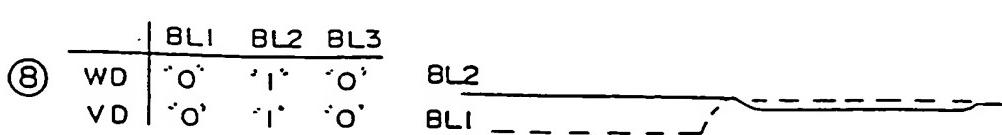


FIG. 69(a)

	BL1	BL2	BL3
WD	'1'	'0'	'1'
VD	'1'	'1'	'1'

FIG. 69(b)

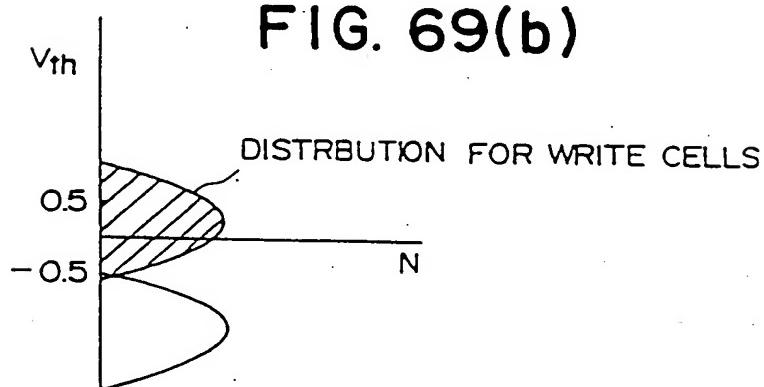


FIG. 69(c)

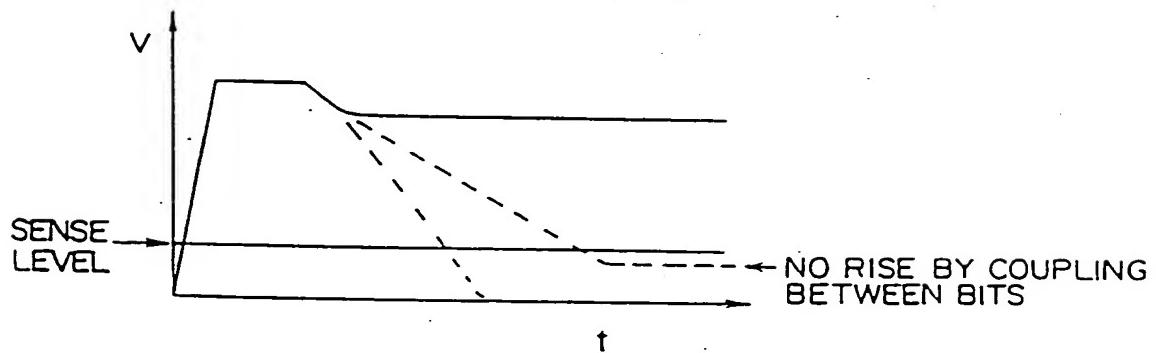


FIG. 70(a)

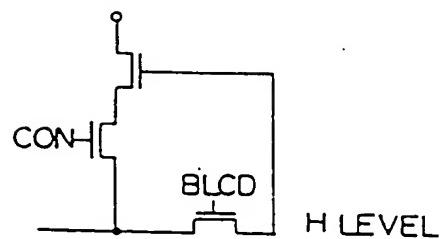


FIG. 70(b)

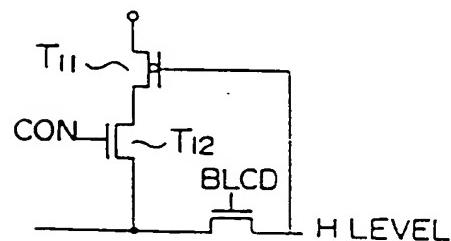
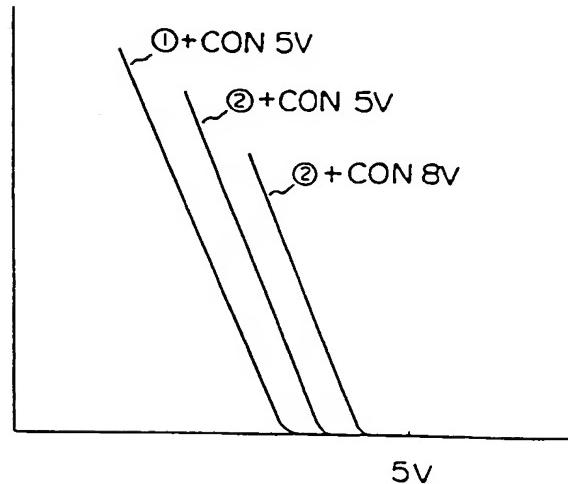


FIG. 70(c)



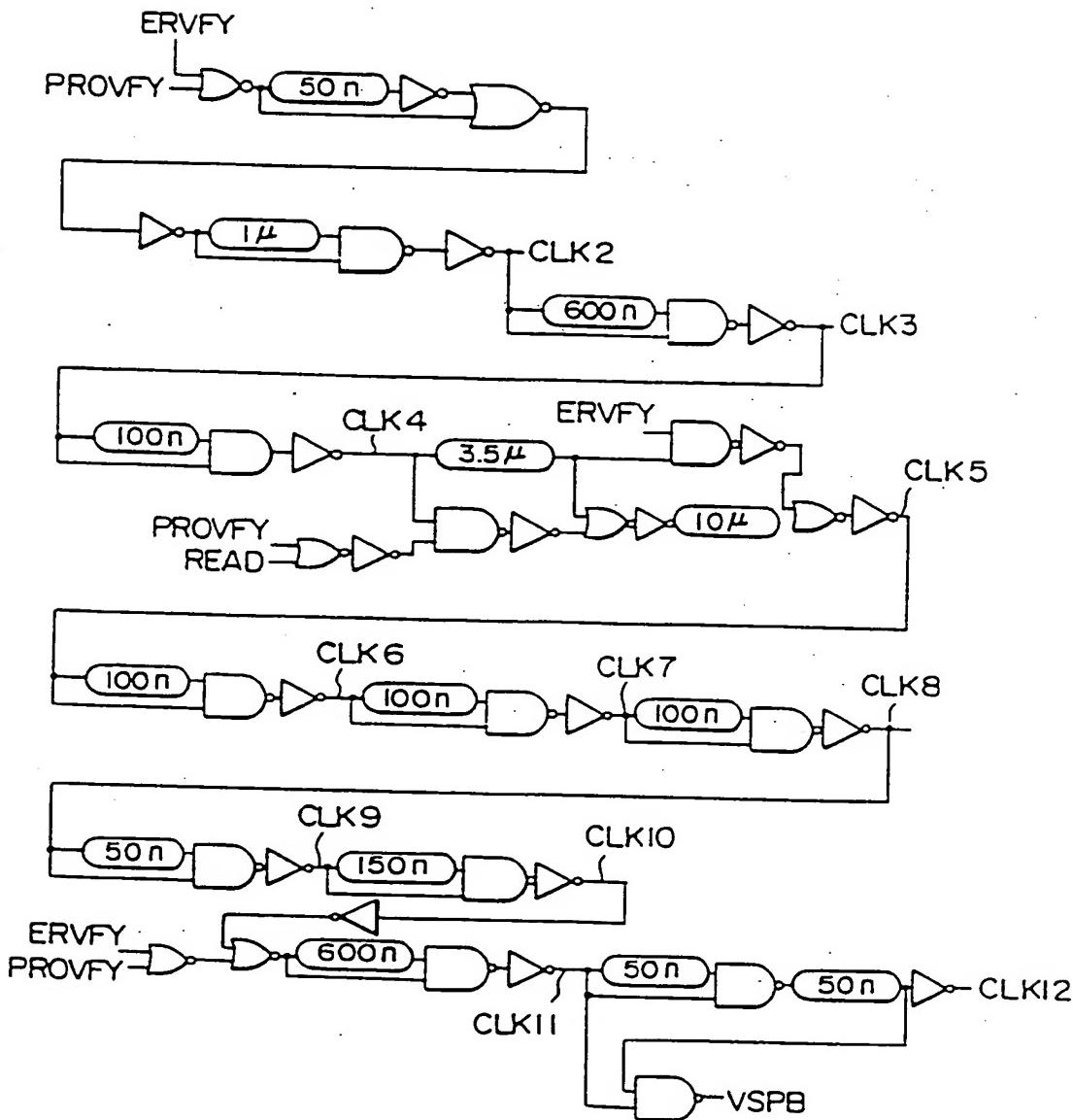


FIG. 71

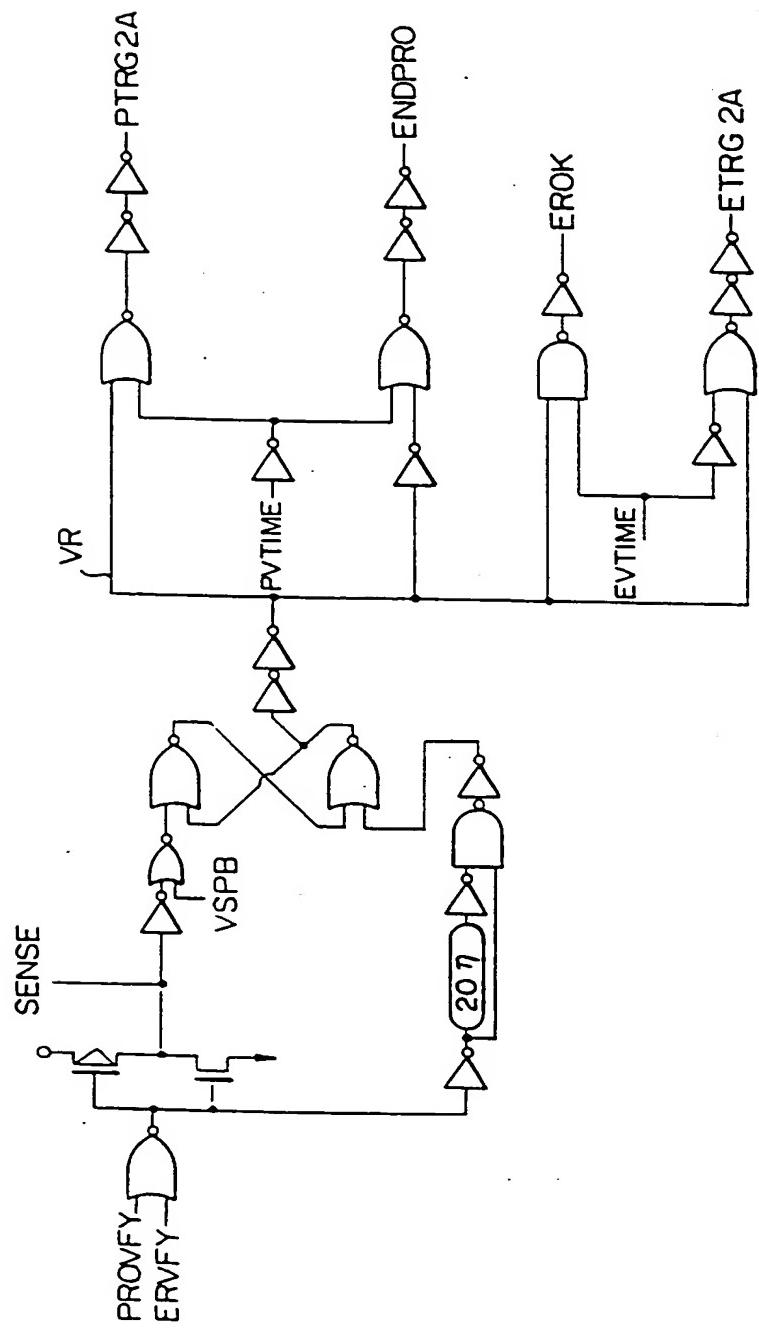


FIG. 72

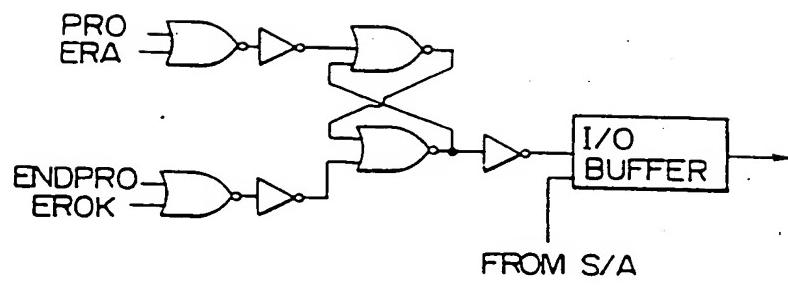


FIG. 73

FIG. 74(a)

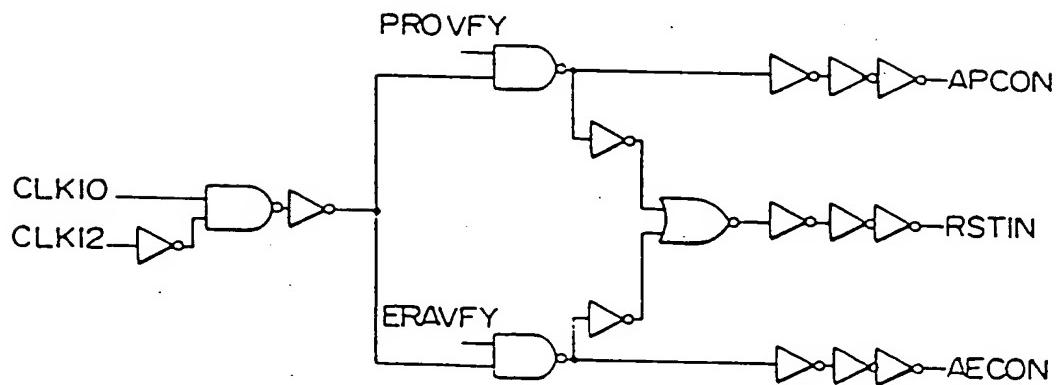


FIG. 74(b)

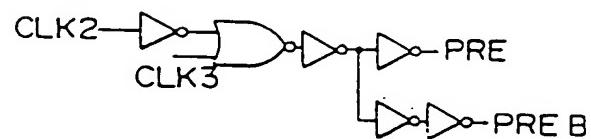
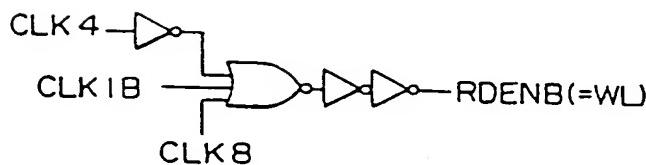


FIG. 74(c)



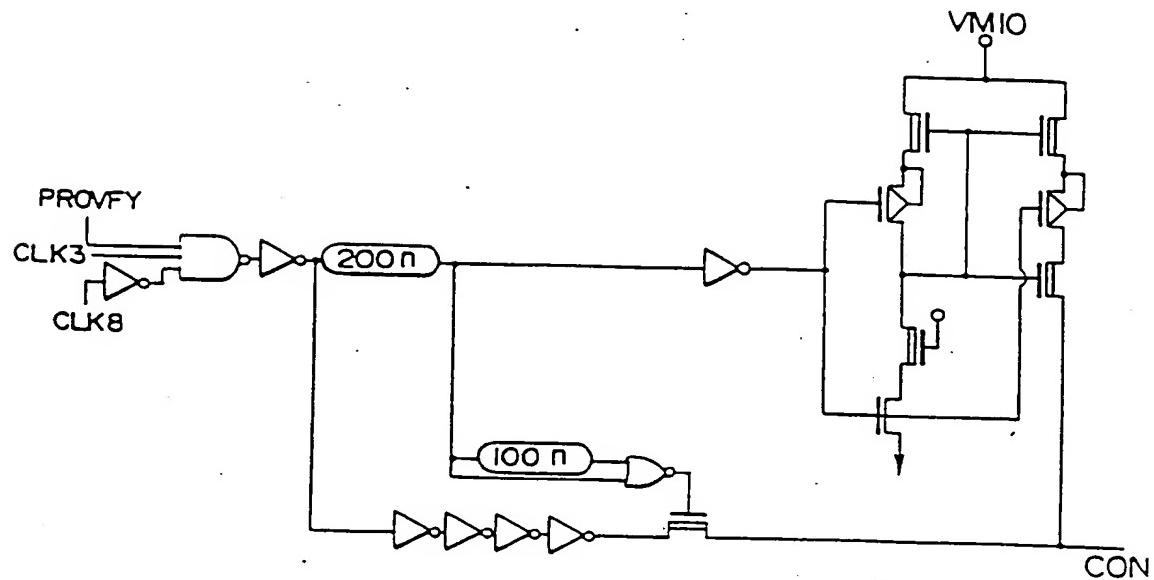


FIG. 75

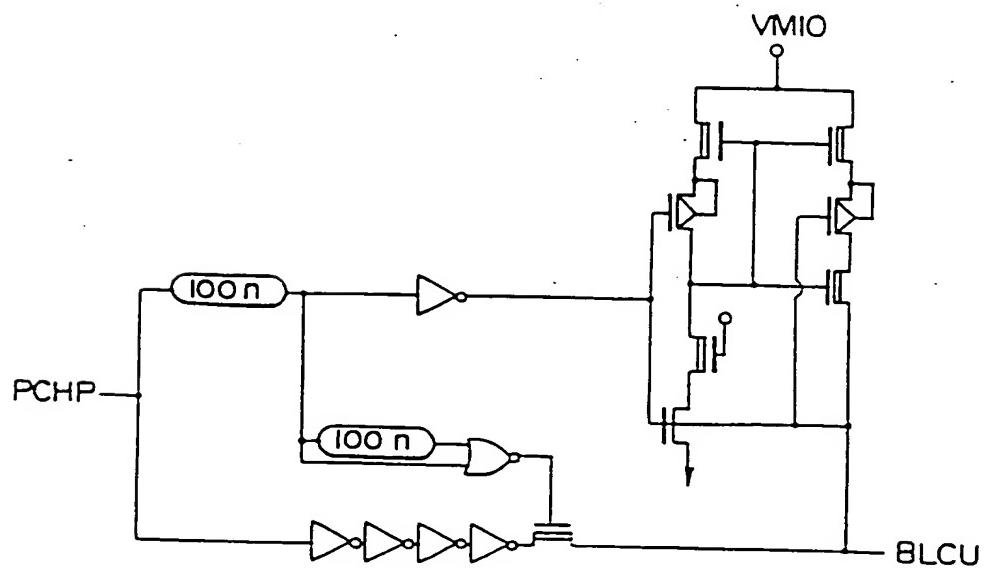


FIG. 76

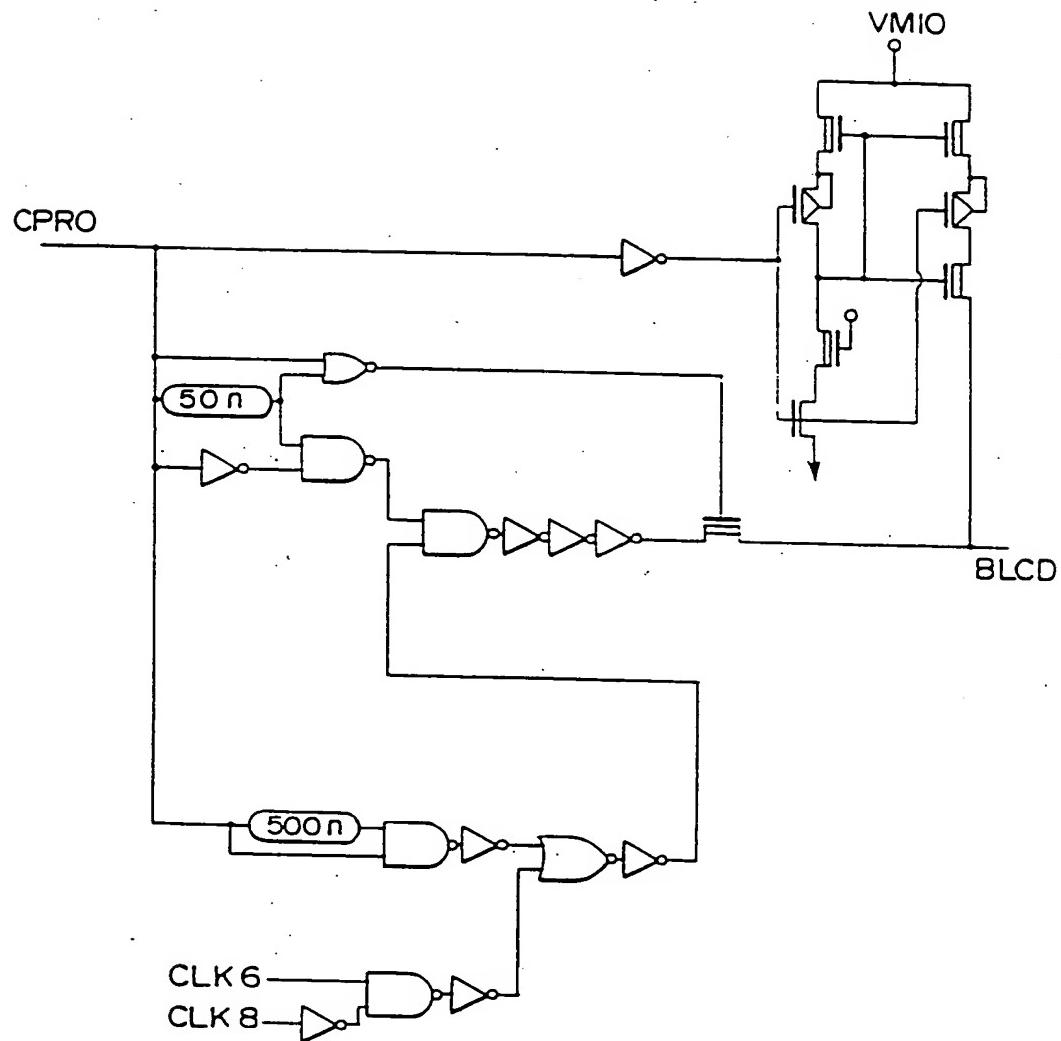


FIG. 77

FIG. 78(a)

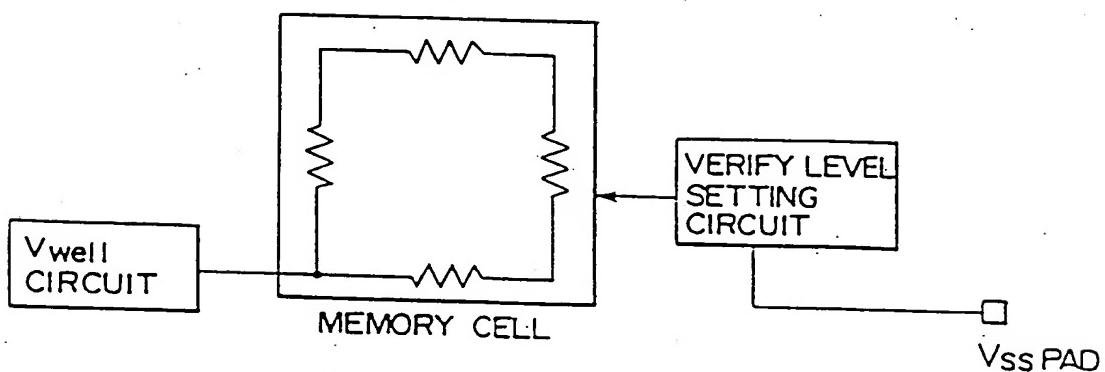
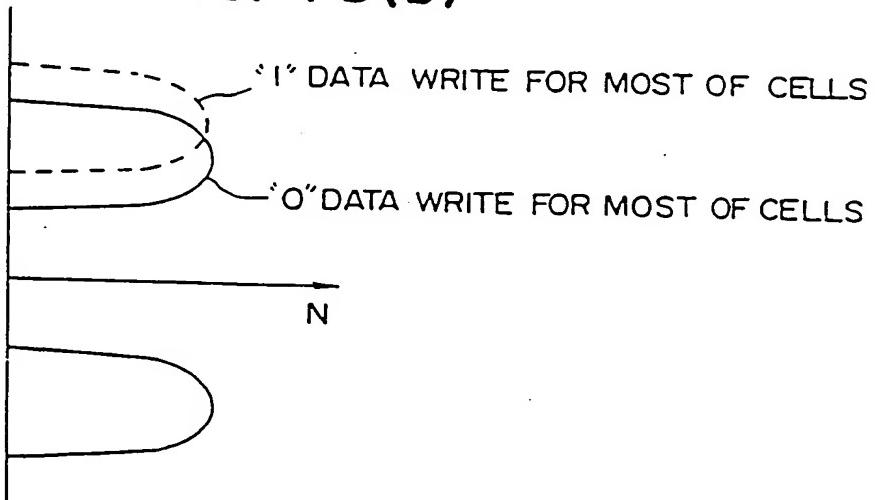


FIG. 78(b)



Title: NON-VOLATILE SEMICONDUCTOR
MEMORY DEVICE AND MEMORY
SYSTEM USING THE SAME
Inventor(s): Tomoharu TANAKA et al.
DOCKET NO.: 016887-1102

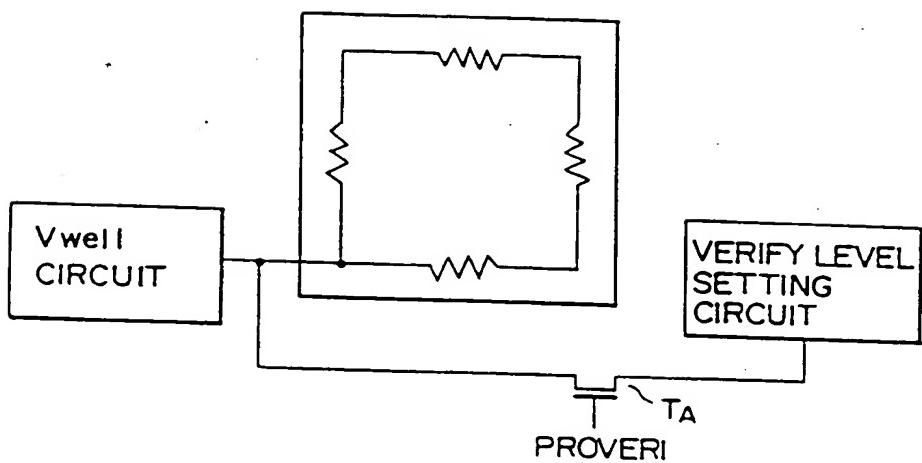


FIG. 79

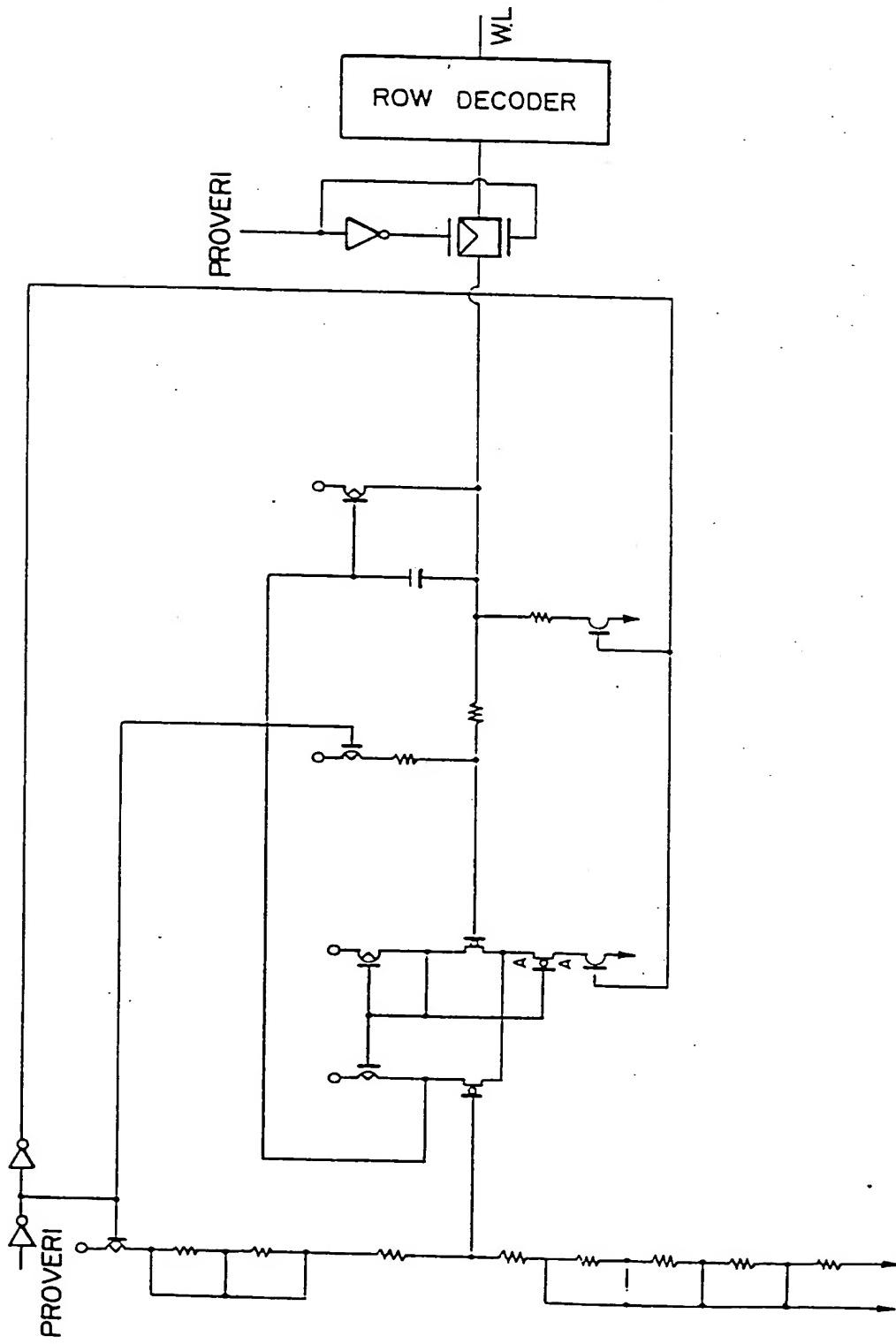


FIG. 80

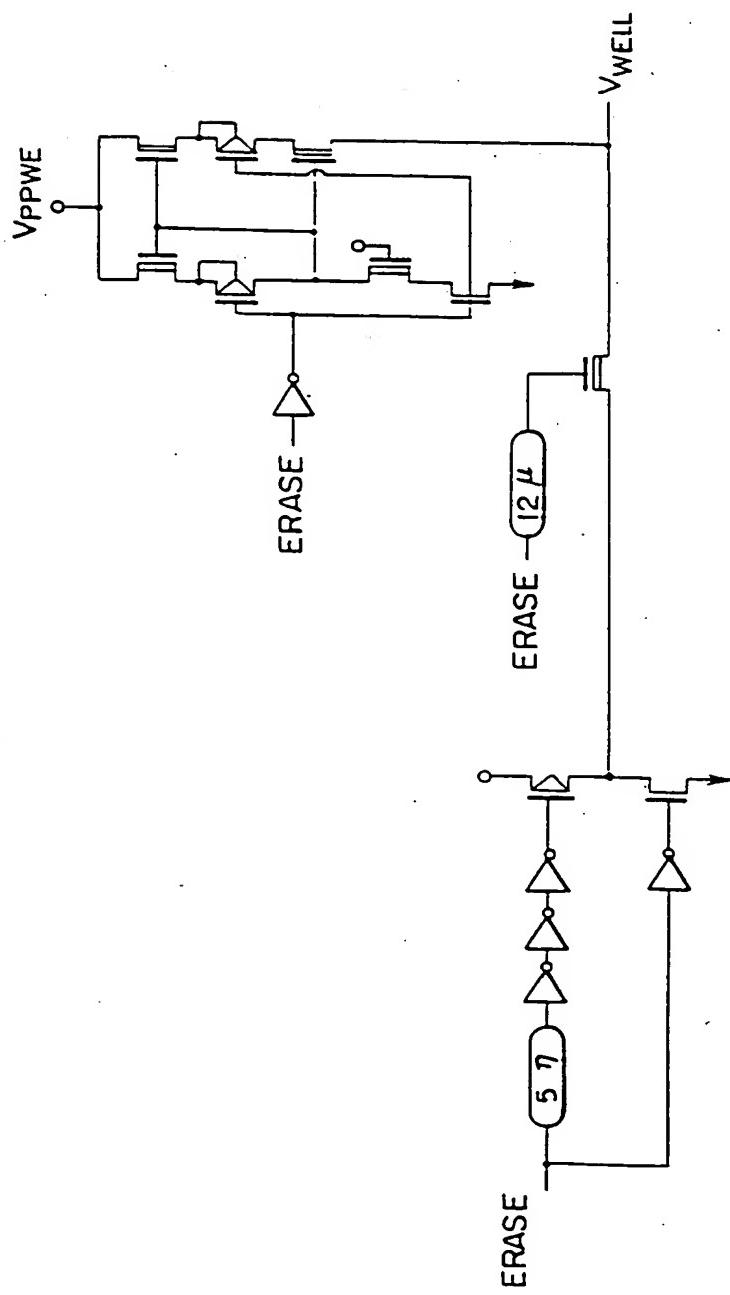


FIG. 81

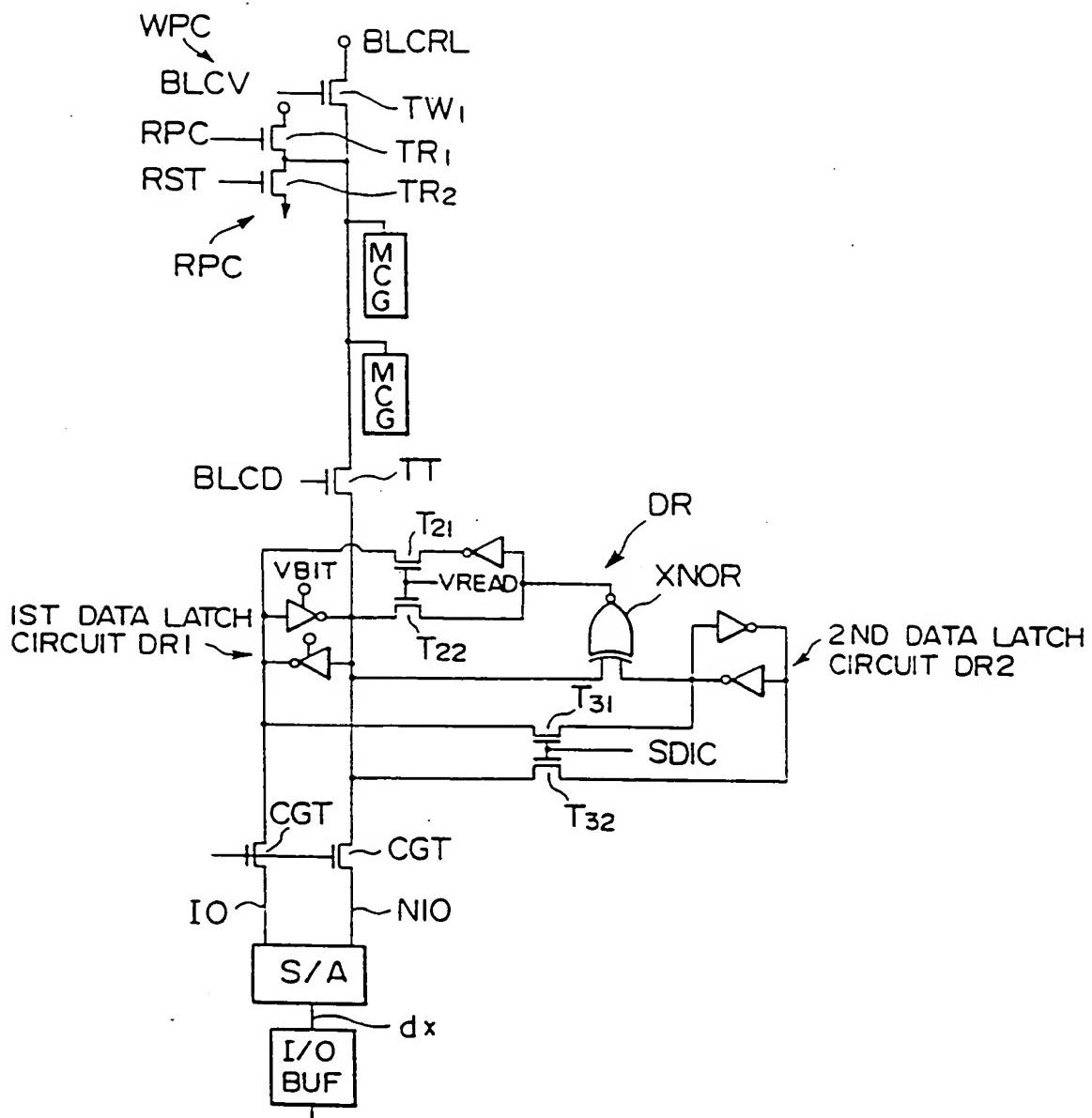


FIG.82

WRITE DATA	0	0	1	1
VERIFY DATA	0	1	0	1
OUTPUT DATA AFTER COMPAR- ISON	0	1	1	0

FIG.83

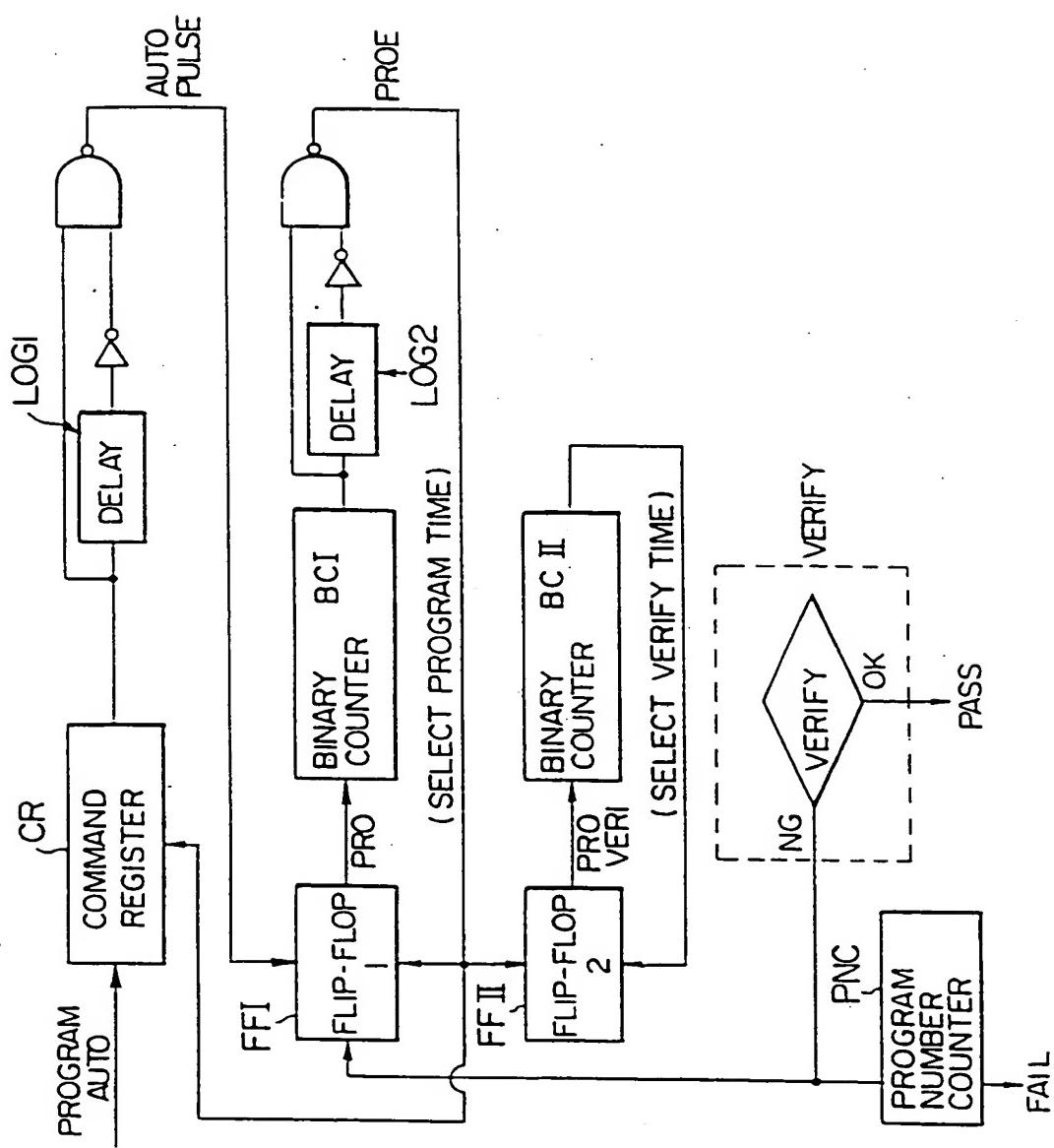


FIG. 84

Title: NON-VOLATILE SEMICONDUCTOR
MEMORY DEVICE AND MEMORY
SYSTEM USING THE SAME
Inventor(s): Tomoharu TANAKA et al.
DOCKET NO.: 016887-1102

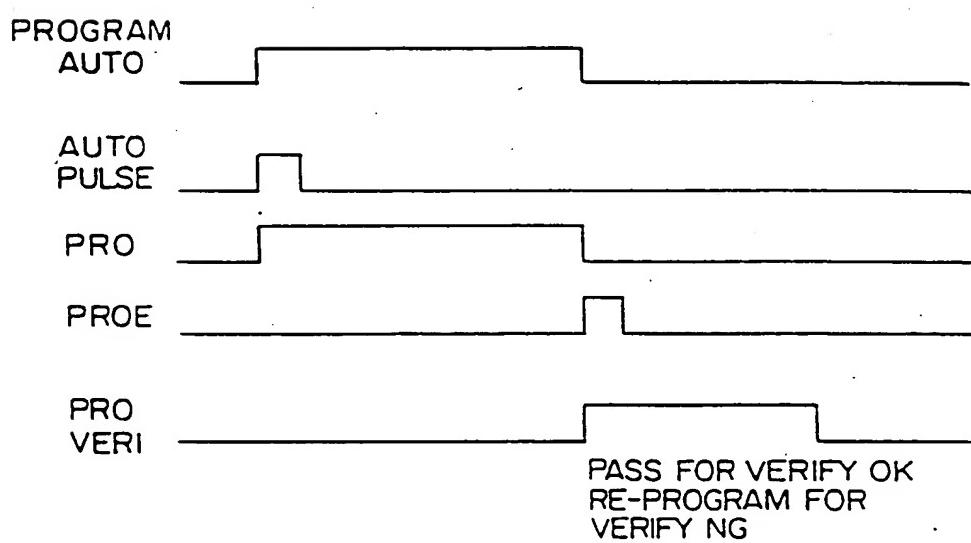


FIG. 85

PROGRAM & PROGRAM VERIFY OPERATIONS

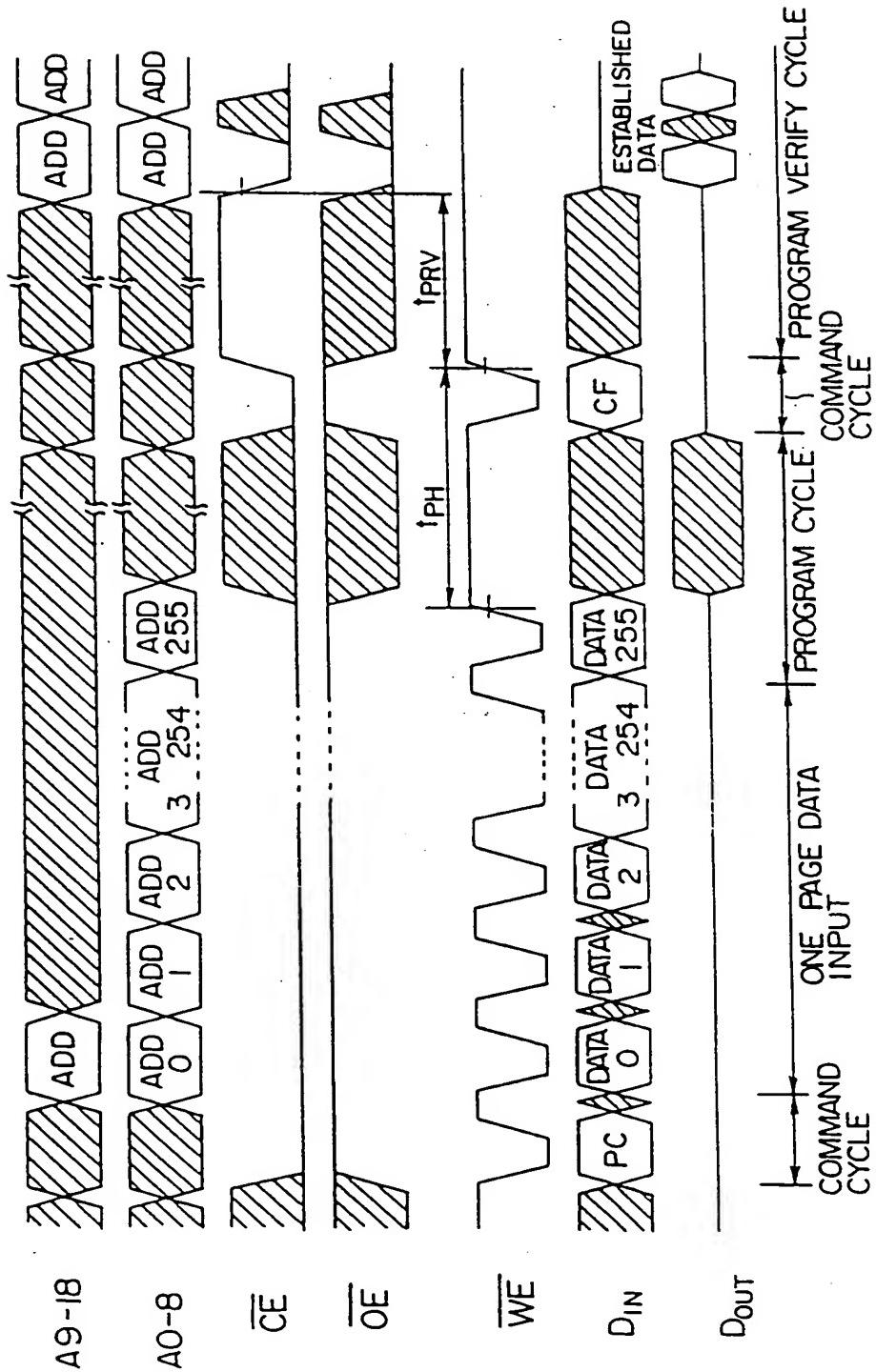


FIG. 86

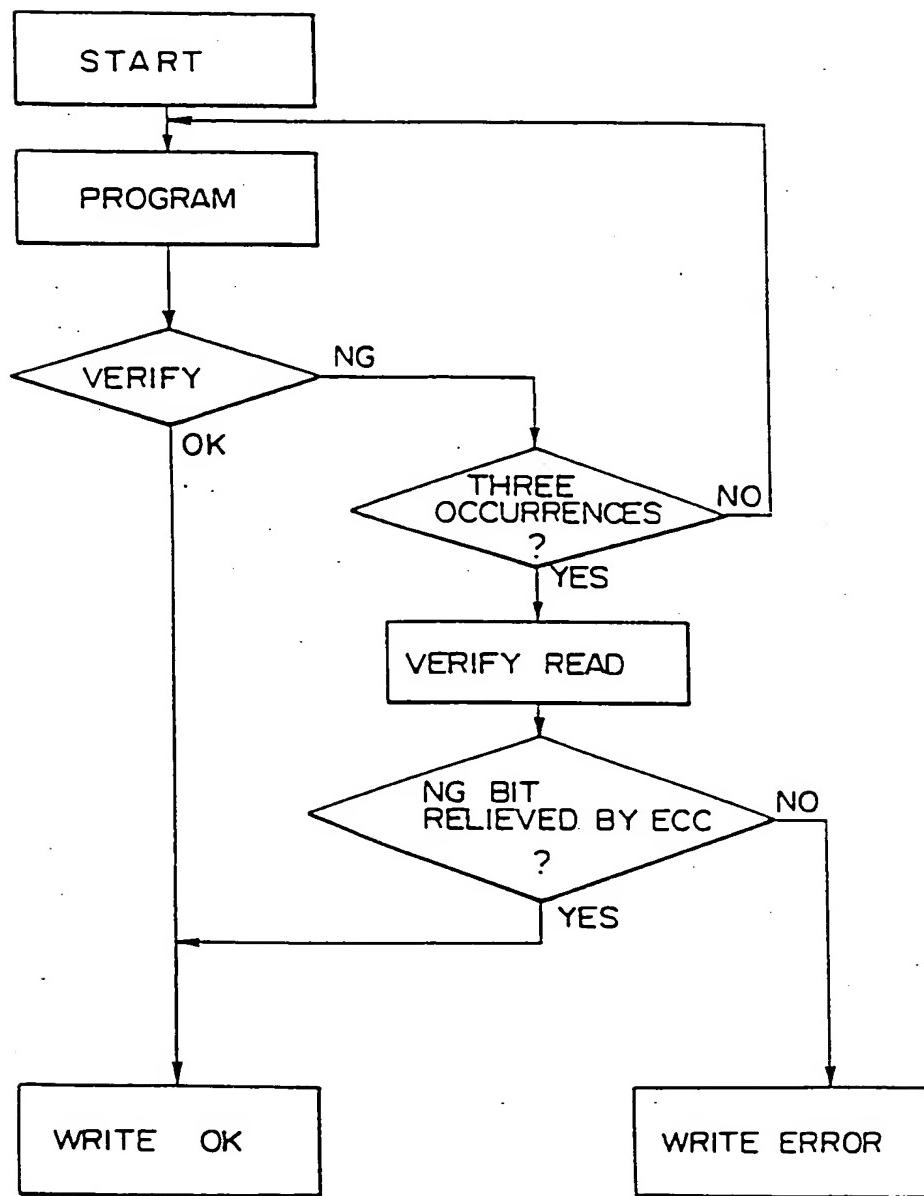


FIG. 87

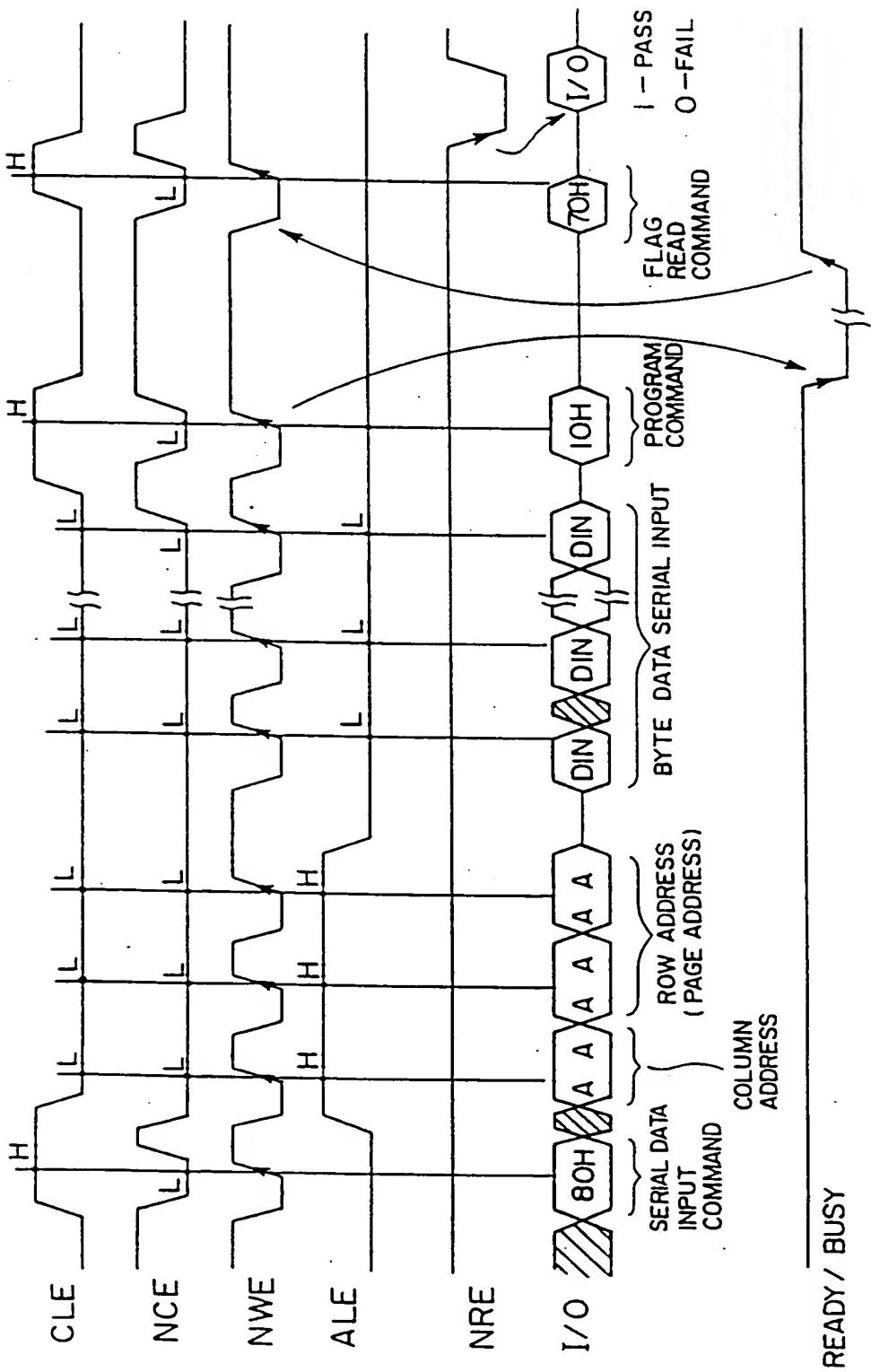


FIG. 88

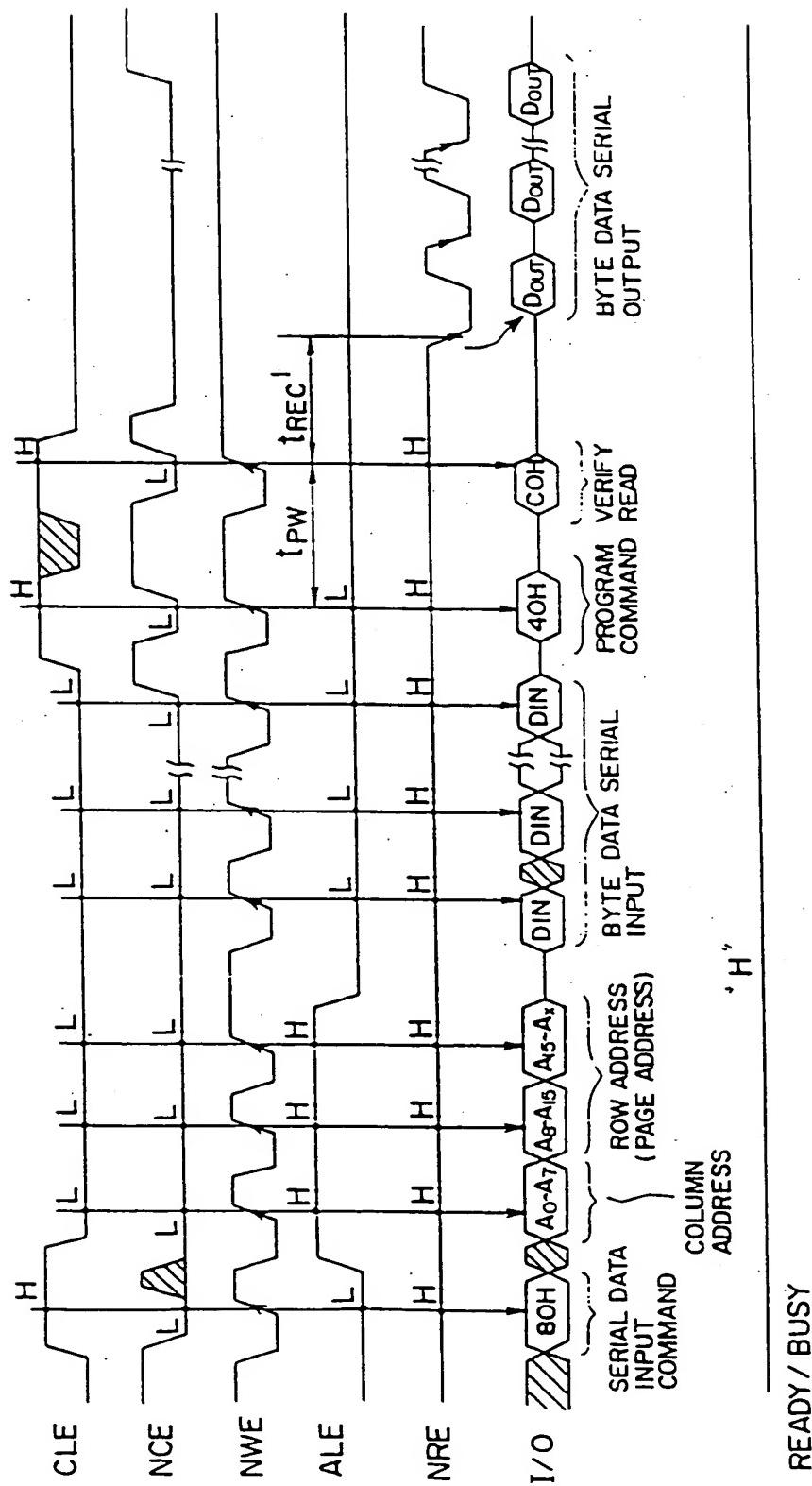


FIG. 89

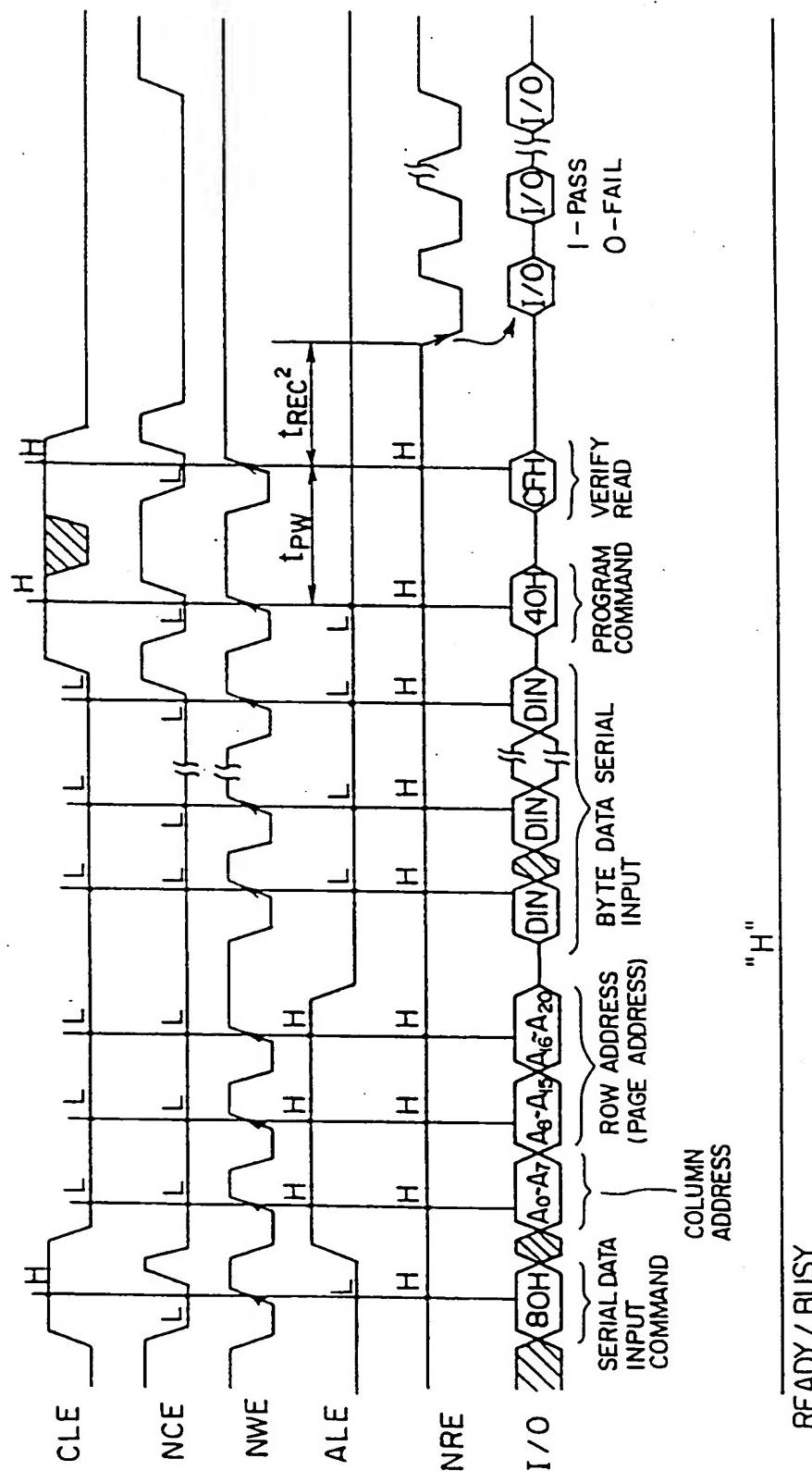


FIG. 90

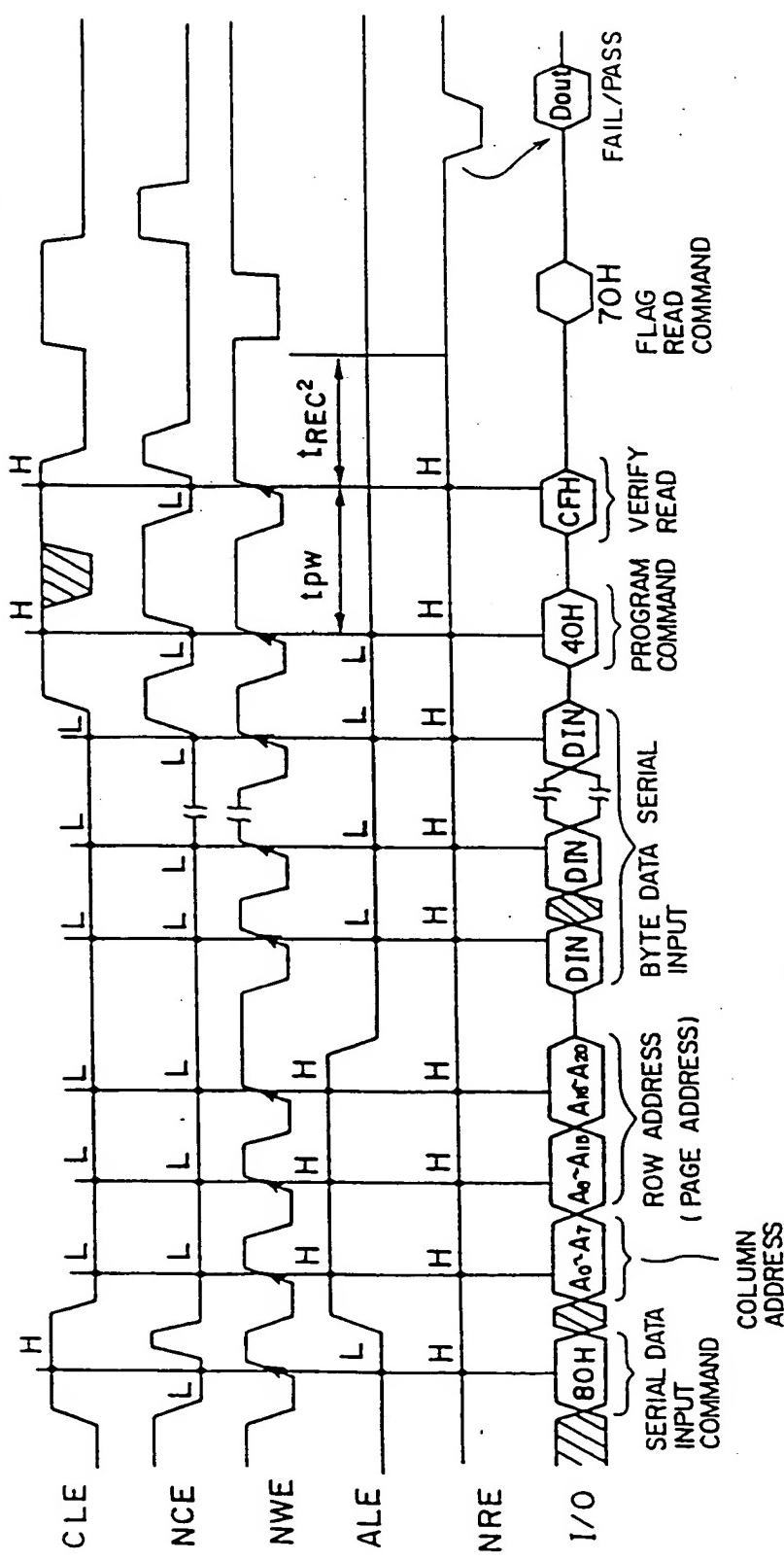


FIG. 9I

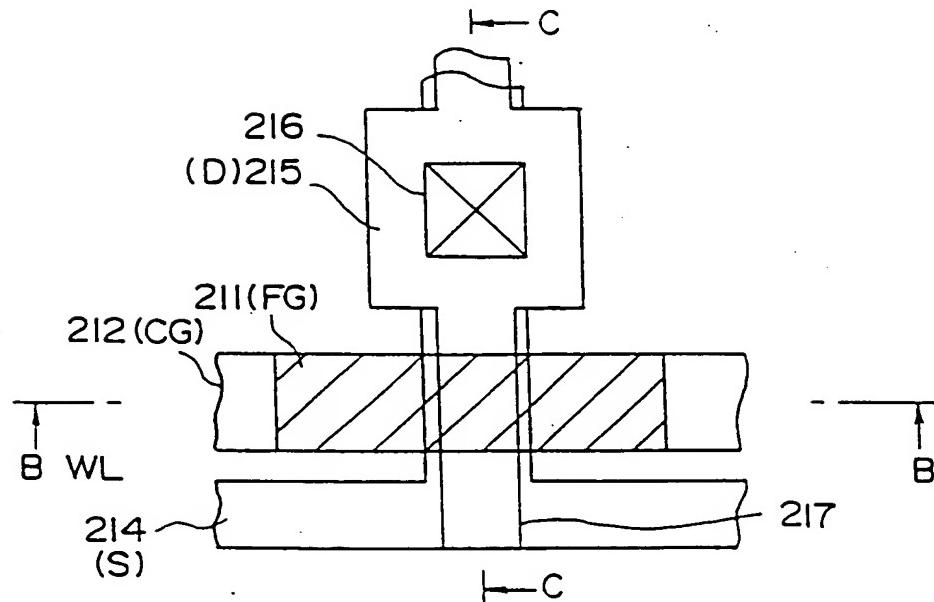


FIG. 92

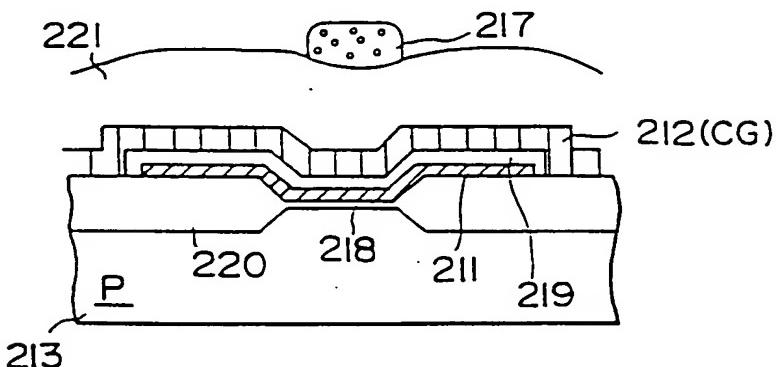


FIG. 93

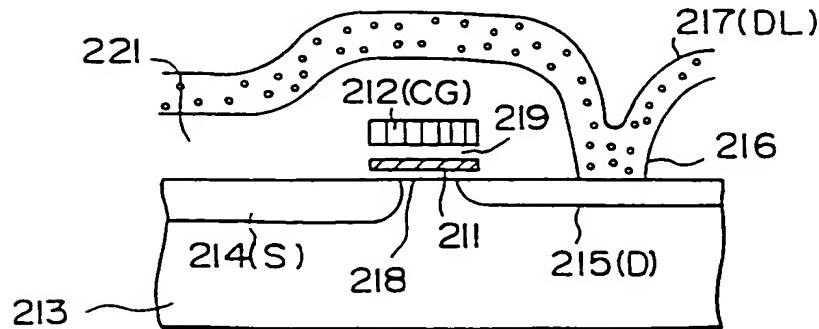


FIG. 94

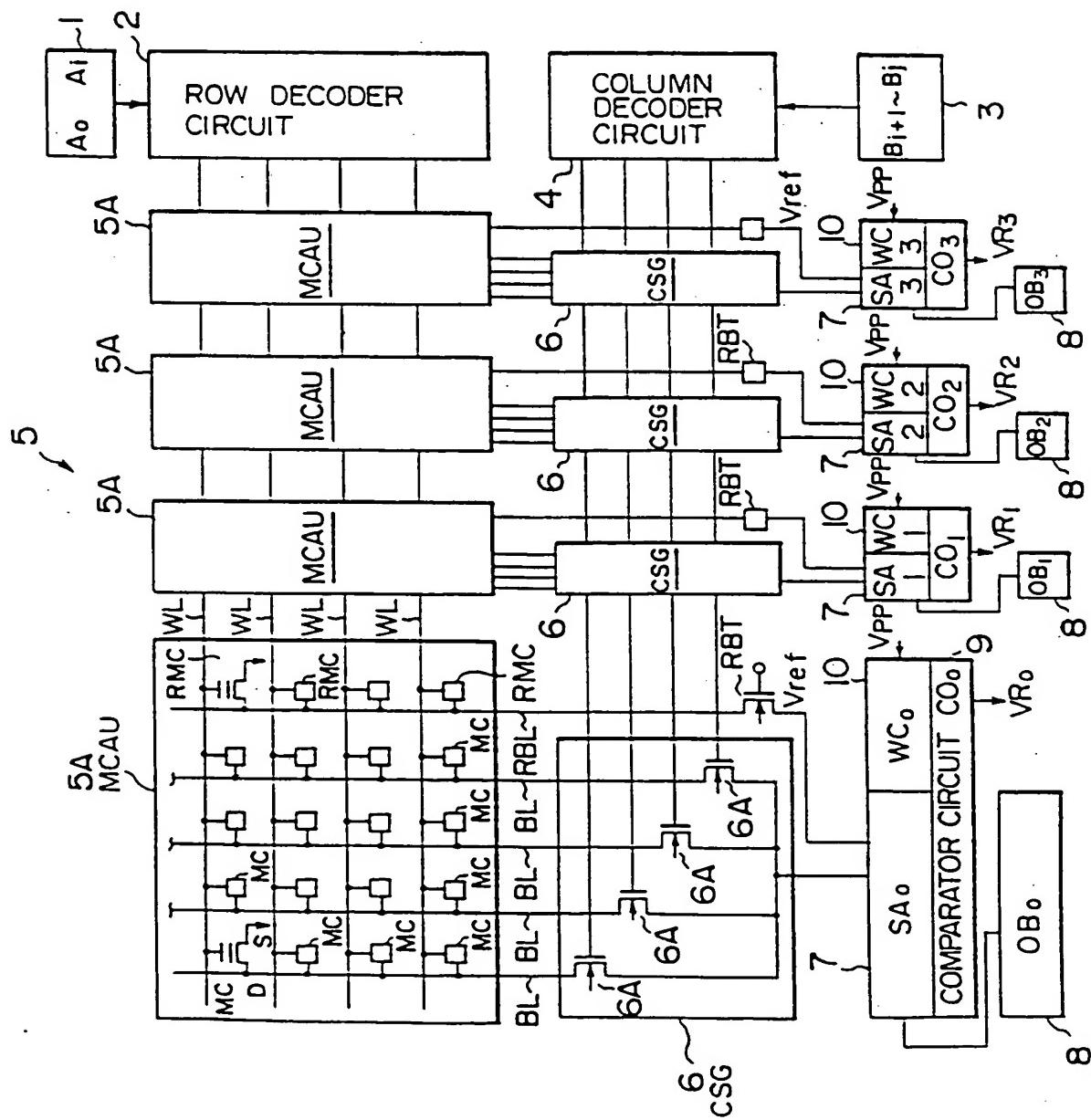


FIG. 95

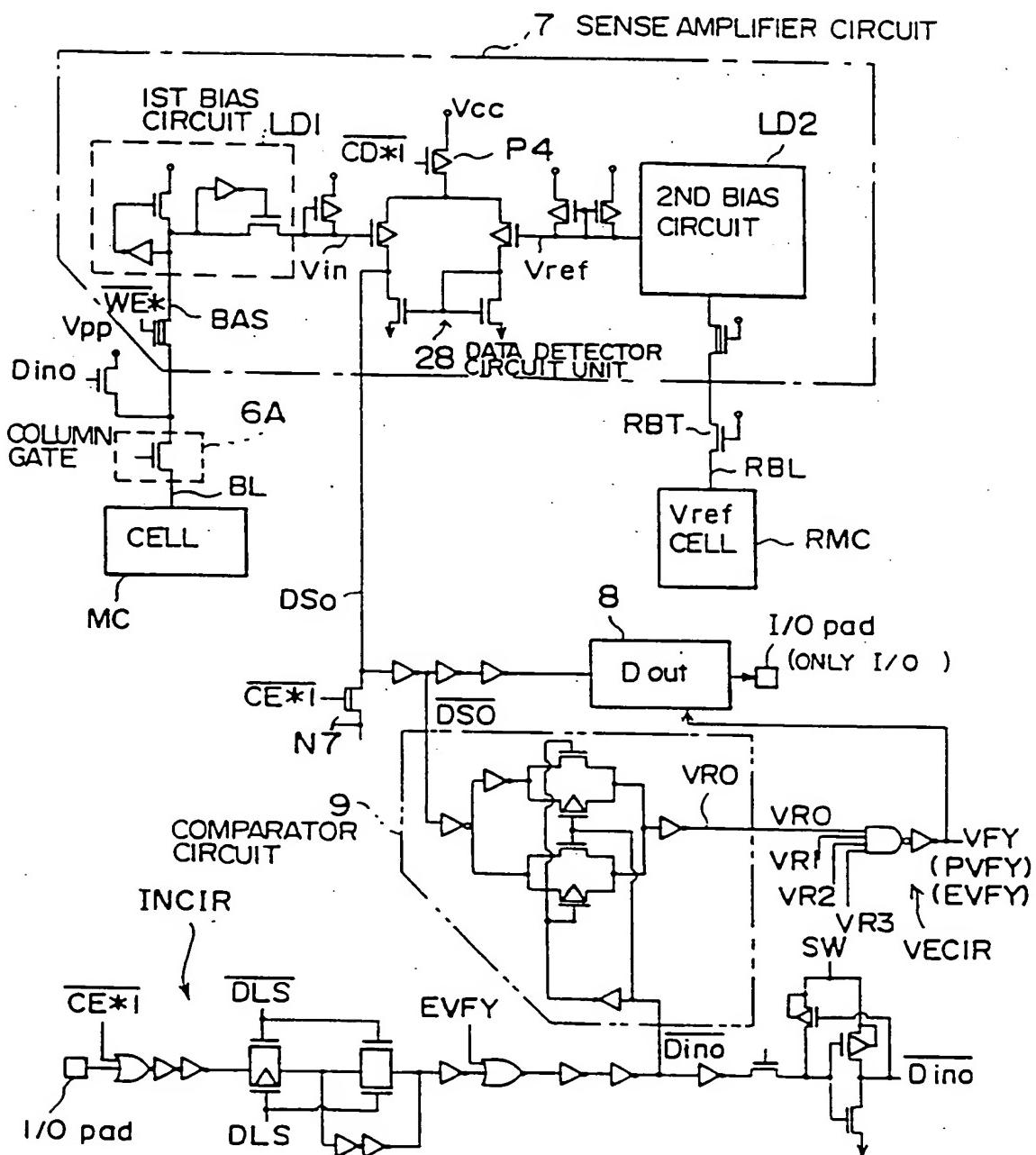


FIG. 96

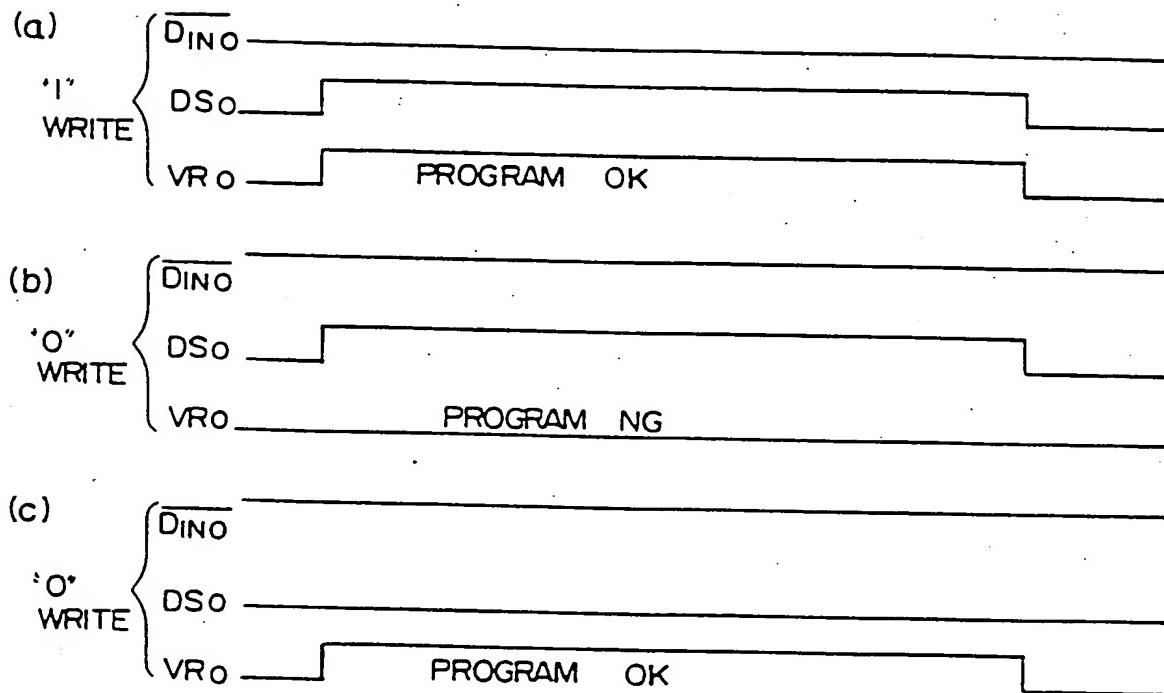


FIG. 97

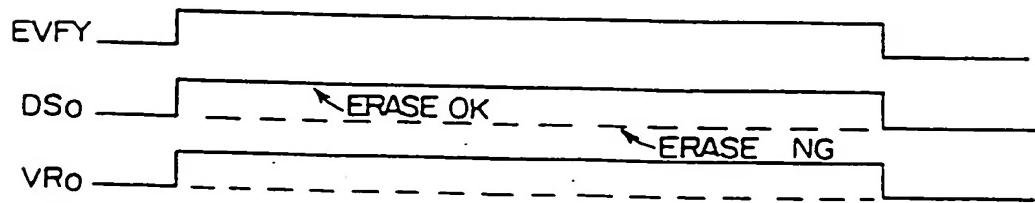


FIG. 98

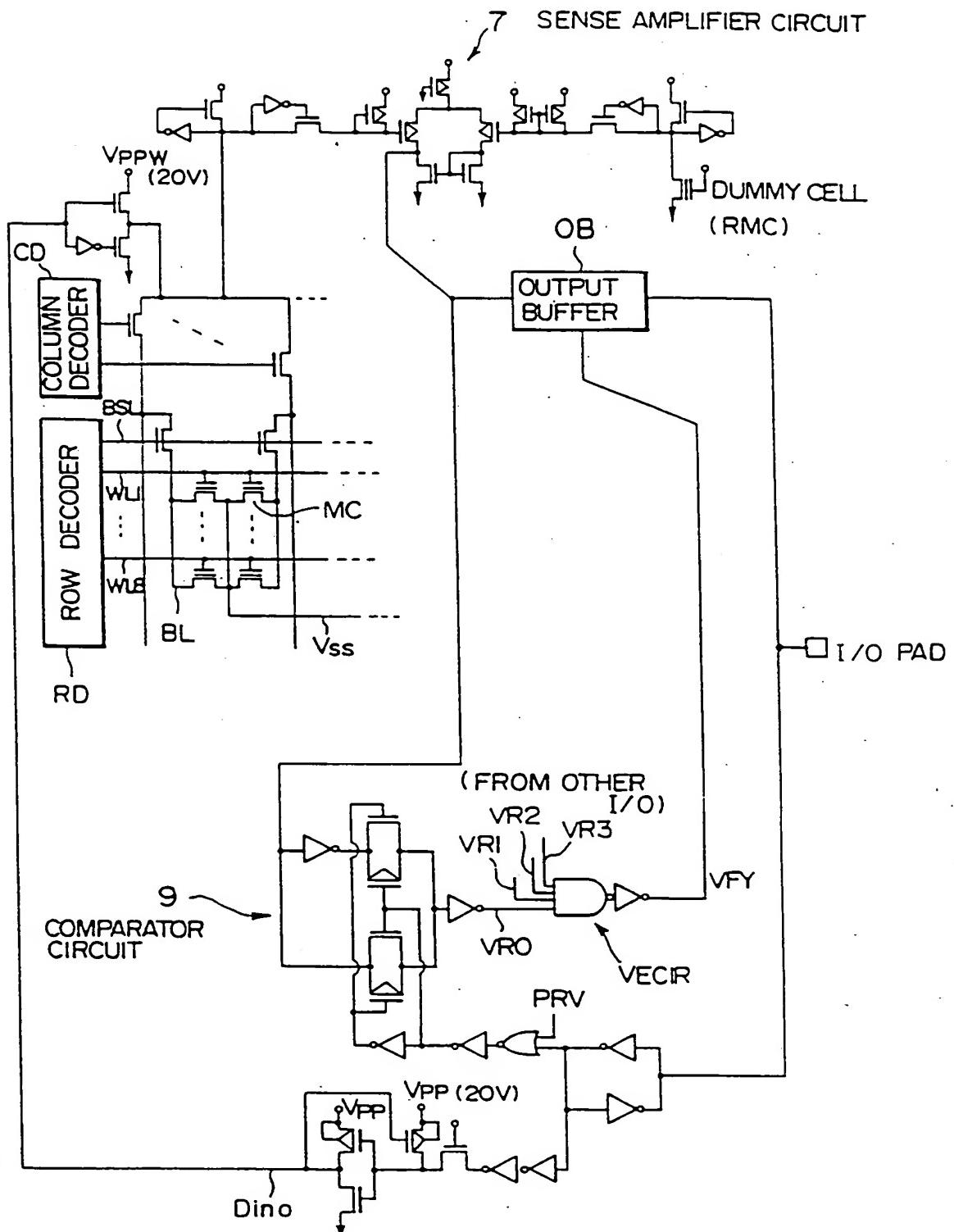


FIG. 99

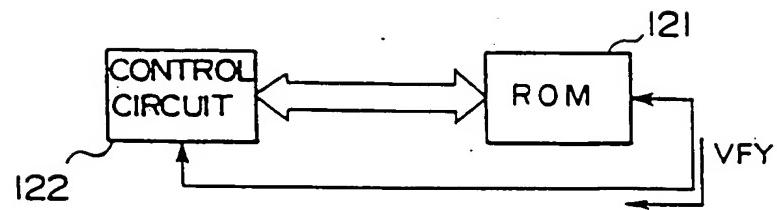


FIG. 100

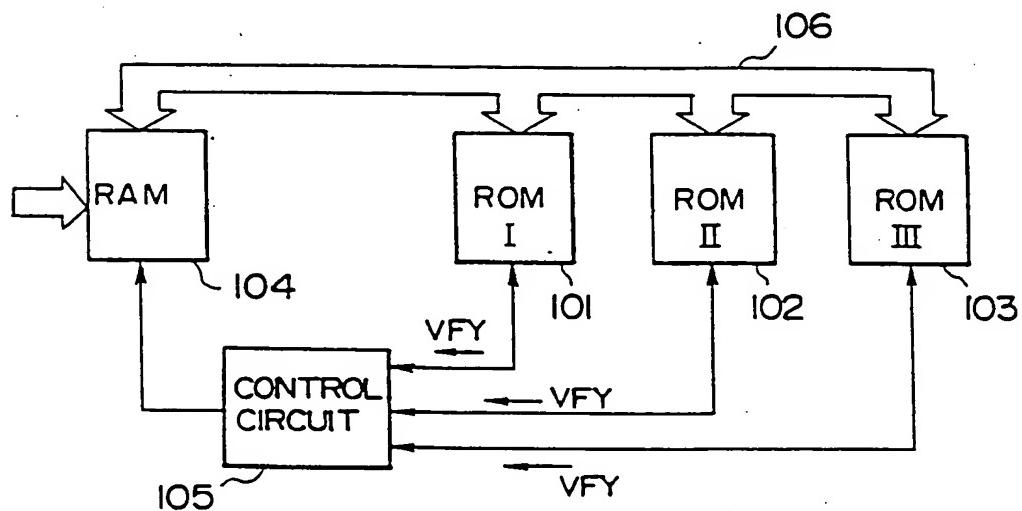


FIG. 101

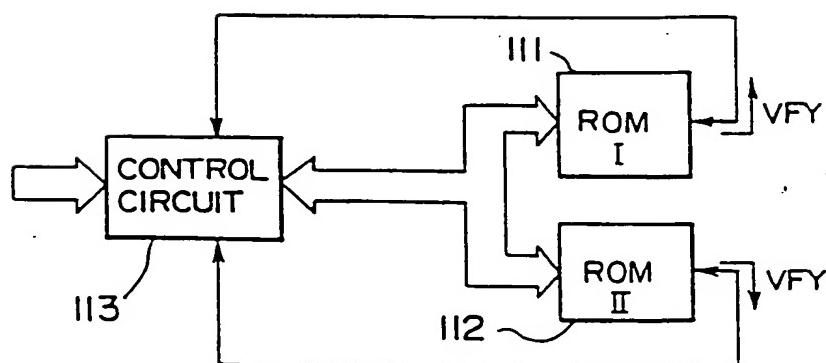


FIG. 102